MT90500

Multi-Channel AAL1 SAR

Preliminary Information

ISSUE 3 April 1998

Ordering Information

MT90500AL 240 Pin Plastic QFP

-40 to +85 C

Features

- AAL1 Segmentation and Reassembly device compatible with Structured Data Transfer (SDT) as per ANSI T1.630 and ITU I.363 standards
- Transports 64kbps and n x 64kbps traffic over ATM AAL1 cells (also over AAL5 or AAL0)
- Simultaneous processing of up to 1024 bidirectional Virtual Circuits
- Flexible aggregation capabilities (n x 64) to allow any combination of 64 kbps channels while maintaining frame integrity (DS0 grooming)
- Support for clock recovery - Adaptive Clock Recovery or external
- Primary UTOPIA port (Level 1, 25 MHz) for connection to external PHY devices with data throughput of up to 155 Mbps
- Secondary UTOPIA port for connection to an external AAL5 SAR processor, or for chaining multiple MT90500 devices
- 16-bit microprocessor port, configurable to Motorola or Intel timing
- TDM bus provides 16 bidirectional serial TDM streams at 2.048, 4.096, or 8.192 Mbps for up to 2048 TDM 64 kbps channels
- Compatible with ST-BUS, MVIP, H-MVIP and SCSA interfaces
- Supports master and slave TDM bus clock operation
- Loopback function at TDM bus interface
- Local TDM bus provides clocks, input pin and output pin for 2.048 Mbps operation
- Master clock rate up to 60 MHz
- Dual rails (3.3V for power minimization, 5V for standard I/O)
- IEEE1149 (JTAG) interface

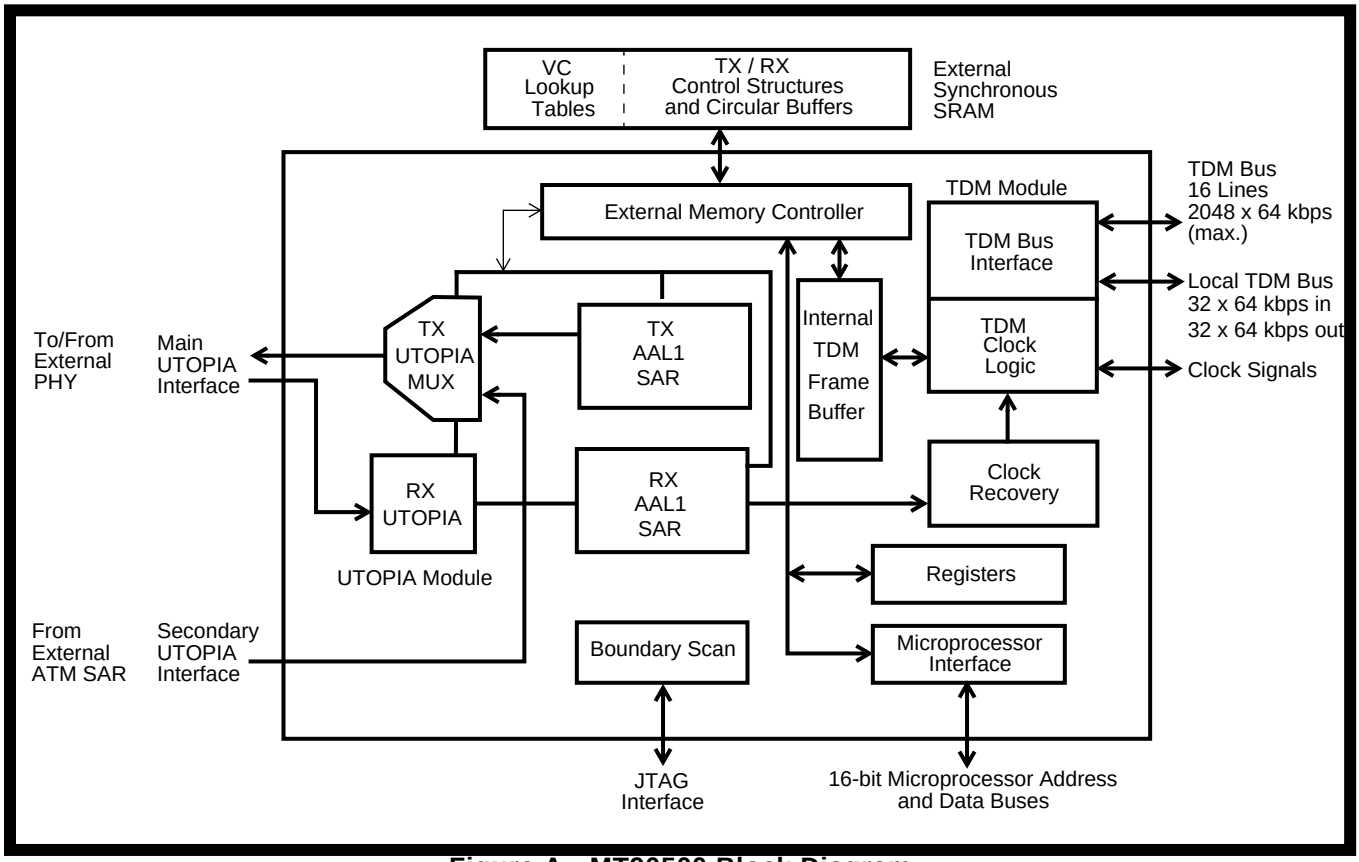

Figure A - MT90500 Block Diagram

Applications

- B-ISDN (Broadband ISDN) systems requiring flexible n x 64kbps transport
- Connecting TDM backplane to TDM backplane over ATM network (GO-MVIP MC4, or other)
- Systems requiring ANSI T1.630 Structured Data Transfer services for 1 to 122 TDM channels per VC
- Systems requiring ITU-T I.363.1circuit transport over Structured Data Transfer for 1 to 96 TDM channels per VC
- Systems requiring AF-VTOA-0078.000 (ATM Forum CES v2.0) “N x 64 Basic Service”
- Systems requiring AF-VTOA-0083.000 Voice and Telephony over ATM (CBR-AAL5).
- Mapping between CBR-AAL0, CBR-AAL5, and AAL1
- Mapping between partially-filled cells and full cells
- Mapping between single-voice cells and n x 64 cells
- ATM uplink for expansion of COs, PBXs, or open switching platforms using an adjunct ATM switch
- ATM Public Network access for PBX or CO
- ATM Edge Switches and CPE Integrated-Access over ATM
- TDM traffic transfer over an asynchronous cell bus

Description

The MT90500 Multi-Channel AAL1 SAR is a highly integrated solution which allows systems based on a telecom bus to be interfaced to ATM networks using ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 5 (AAL5) and ATM Adaptation Layer 0 (AAL0). The MT90500 can be connected directly to a ST-BUS time division multiplexed (TDM) backplane containing up to 1024 full duplex 64kbps channels. Up to 1024 bi-directional ATM VC connections can be simultaneously processed by the MT90500 AAL1 SAR device.

On the synchronous TDM bus side, the MT90500 device interfaces with sixteen bidirectional ST-BUS serial links operating at 2.048, 4.096 or 8.192 Mbps. TDM bus compatibility with MVIP-90, H-MVIP, and SCSA interfaces is also provided.

On the ATM interface side, the MT90500 device meets the ATM Forum standard UTOPIA Bus Level 1. This supports connection to a range of standard physical layer (PHY) transceivers.

The MT90500 provides a built-in UTOPIA multiplexer which allows external ATM cells to be multiplexed with internally-generated cells in the transmit direction. This feature can be used to connect another MT90500 (to expand the TDM bandwidth of the system to 4096 TDM channels), or to connect an external AAL5 SAR (to multiplex non-CBR ATM cell traffic with the MT90500 CBR stream).

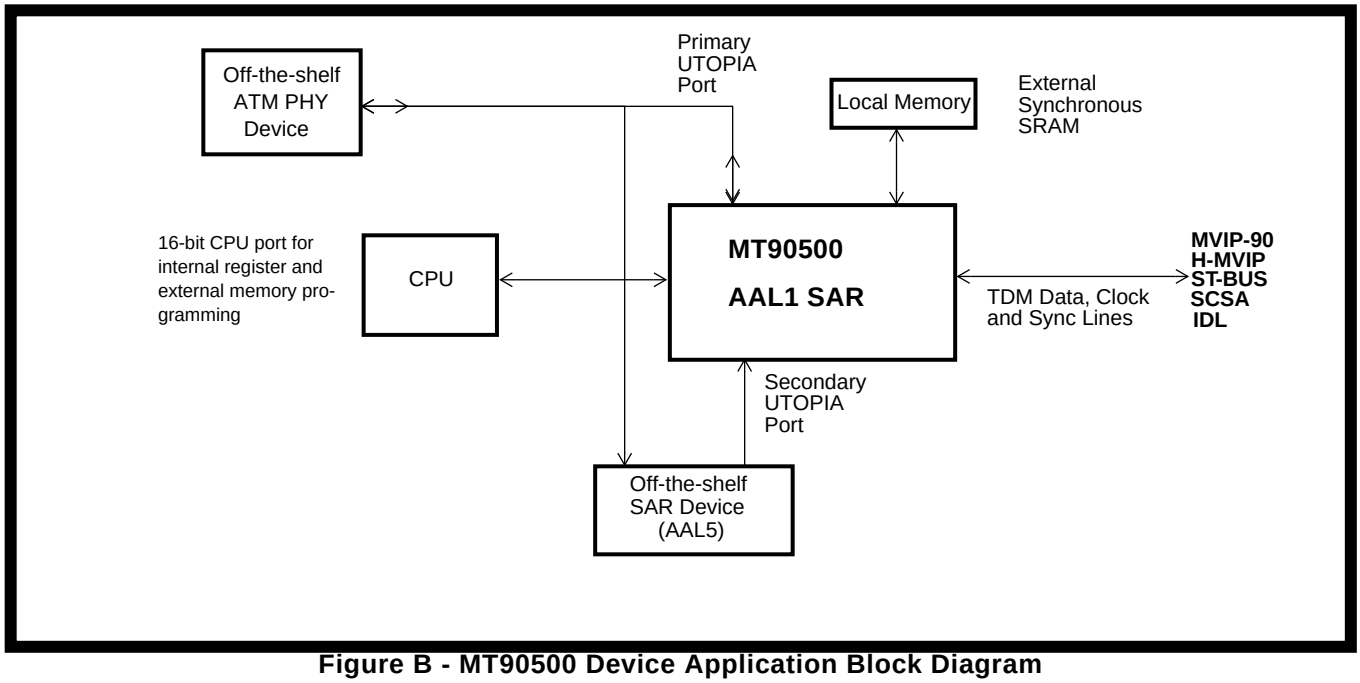

Figure B - MT90500 Device Application Block Diagram

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1. Introduction

1.1 Functional Overview

The Mitel MT90500 Multi-Channel AAL1 SAR bridges a standard isochronous TDM (Time Division Multiplexed) backplane to a standard ATM (Asynchronous Transfer Mode) bus. On the TDM bus side, the MT90500 can interface to 16 bidirectional TDM bus links operating at 2.048, 4.096 or 8.192 Mbps (compatible with MVIP / H-MVIP, SCSA and Mitel ST-BUS). On the ATM interface side, the MT90500 provides the UTOPIA bus standardized by the ATM Forum. The device provides the AAL1 Structured Data Transfer (referred to as SDT from now on in this document) and pointerless Structured Data Transfer mappings defined by ANSI T1.630-1993 and ITU-T I.363. In addition, the MT90500 provides CBR (Constant Bit Rate) mapping of TDM to AAL0, and to AAL5 (CBR-AAL5). In all data transfer formats, the user simply ports the T1/E1, T3/E3, etc. traffic onto the TDM backplane before applying it to the MT90500. As well, the device also supports TDM clock recovery using adaptive or external clock recovery.

In the receive direction, ATM cells with VCs destined for the MT90500 are extracted from the UTOPIA bus and sent toward the TDM interface. In the transmit direction, the MT90500 provides multiplexing capabilities at the UTOPIA interface to allow the use of an external AAL5 SAR device, or multiple MT90500 devices. This is useful when CBR data and VBR/ABR/UBR data traffic must be transmitted from the local node on the same physical link. As well, the ability to multiplex internal AAL1 cells with external AAL5 cells can be used to interleave associated signalling cells and control messages with the AAL1 CBR traffic.

The MT90500 also offers some internal support for non-CBR data traffic. If the application's signalling (non-CBR) data throughput is not high, the MT90500 can transmit and receive AAL5 (or other non-CBR data) to / from a pair of FIFOs. This requires the microprocessor to perform SAR functions via software, but may remove the requirement for an external data SAR. Alternatively, if standard AAL5 signalling is not required by the system, the user can use some TDM channels for HDLC or proprietary signalling.

Segmentation and reassembly of TDM data to / from ATM cells is highly flexible. The MT90500 allows the user to select one or more TDM channels to be carried on an ATM logical connection with associated VPI/VCI. The number of TDM channels (1 to 122), the VPI/VCI, the data transfer method (SDT or pointerless Structured Data Transfer), cell partial-fill level, and the AAL (AAL1, CBR-AAL5, or CBR-AAL0) are all programmable. The time slot assignment circuit has 64 kbps granularity and allows a group of TDM channels to be carried on a single ATM logical channel (channel grooming). There is no limitation for distributing n x 64 channels on the TDM bus (i.e. TDM channels on a given VC can be concatenated or dispersed anywhere on the 16 serial data streams).

Up to 1024 bidirectional virtual circuits (VCs) can be handled simultaneously by the internal AAL1 processors. At the maximum TDM rate of 8.192 Mbps, up to 2048 input/output 64 kbps channels are available (1024 bidirectional TDM channels). If the ATM VCs are carrying multiple TDM channels (n x 64), less VCs will be created. The user is given the ability to flexibly define which 64 kbps channels will be converted into ATM VCs. It should be noted that since the MT90500's serial TDM port is fully bidirectional, the ATM logical connections can be defined as full duplex channels (e.g. voice conversation) or one-way connections (e.g. video playback). Using the full duplex capabilities, up to 1024 simultaneous phone calls could be handled by the MT90500.

The MT90500 allows the user to scale the size of the external synchronous memory to suit the application. The external memory's size is influenced by the number of virtual circuits required, the number of TDM channels being handled, and the amount of cell delay variation (CDV) tolerance required for the receive VCs. User-defined lookup tables, data cell FIFOs, and multiple event schedulers also influence the amount of external memory required.

The MT90500 supports two clocking schemes on the TDM bus: clock master and clock slave. In clock master, the MT90500 drives the clocks onto the TDM backplane (the TDM clock is recovered from an incoming ATM VC, or from an external source). In clock slave mode, the MT90500 receives its 8 kHz framing and clocks (4.096, 8.192 or 16.384 MHz) from the TDM backplane, and times its internal functions from that.

Figure 1 on page 10 shows the MT90500 block diagram. The Applications section of this document illustrates several connectivity options with external PHY and SAR devices.

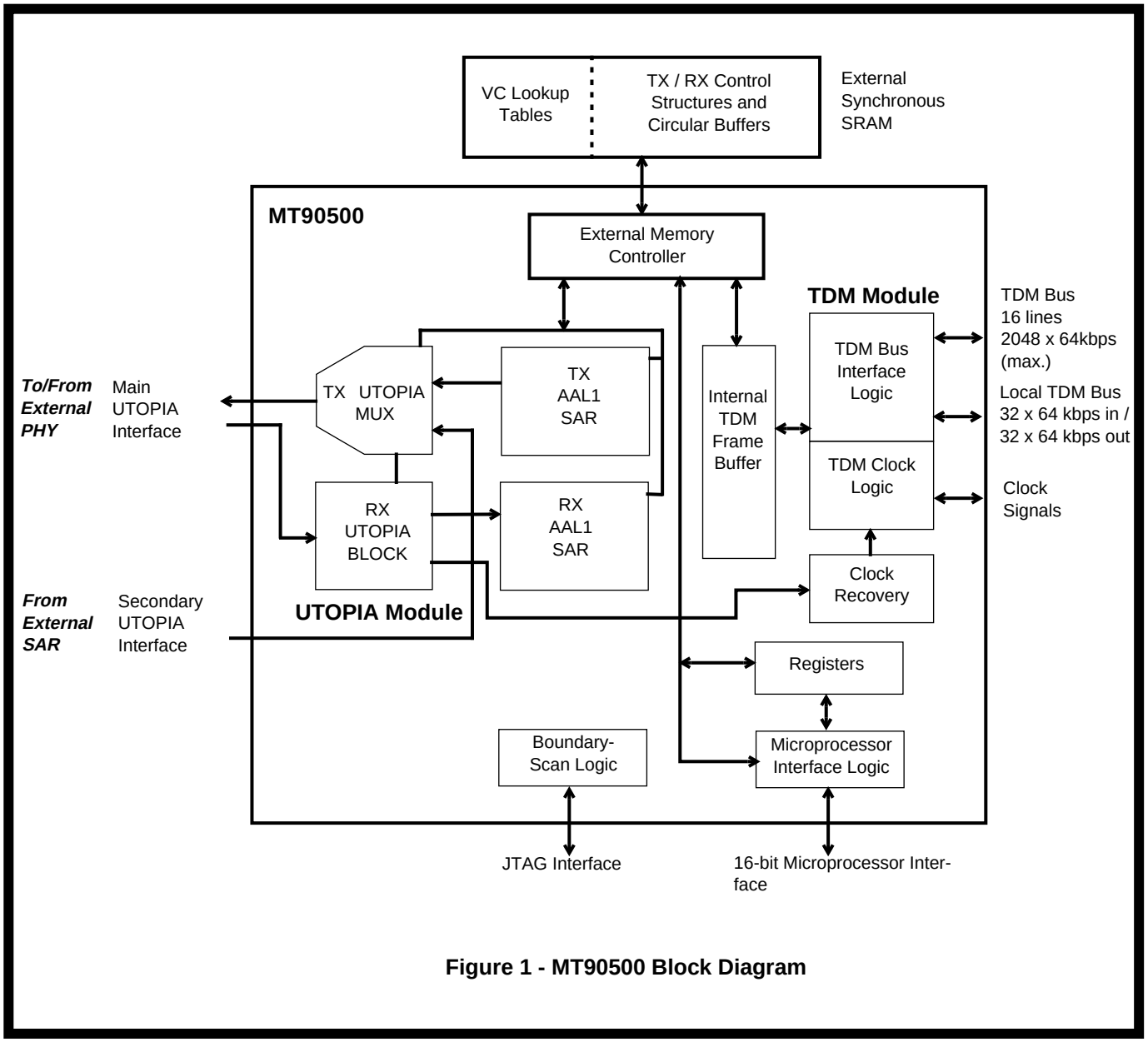


Figure 1 - MT90500 Block Diagram

1.2 Reference Documents

MT90500 Programmer's Manual.

MSAN-171 - TDM Clock Recovery from CBR-over-ATM Links Using the MT90500.

ITU-T Rec. I.363.1, "B-ISDN ATM Adaptation Layer Specification: Type 1 AAL," 08/1996.

ANSI T1.630, "Broadband ISDN - ATM Adaptation Layer for Constant Bit Rate Services Functionality and Specification," 1993.

AF-PHY-0017, "UTOPIA, An ATM-PHY Interface Specification: Level 1, Version 2.01," March 21, 1994.

AF-VTOA-0078.000, "Circuit Emulation Service Interoperability Specification, Version 2.0," Jan. 1997.

AF-VTOA-0083.000, "Voice and Telephony Over ATM to the Desktop Specification, Version 2.0," May 1997.

M. Noorchasm *et al.*, "Buffer Design for Constant Bit Rate Services in Presence of Cell Delay Variation," ATM Forum Contribution 95-1454.

IEEE Std. 1149.1a-1993, "IEEE Standard Test Access Port and Boundary Scan Architecture."

1.3 ATM Glossary

AAL - *ATM Adaptation Layer*; standardized protocols used to translate higher layer services from multiple applications into the size and format of an ATM cell.

AAL0 - native ATM cell transmission; proprietary protocol featuring 5-byte header and 48-byte user payload.

AAL1 - ATM Adaptation Layer used for the transport of constant bit rate, time-dependent traffic (e.g. voice, video); requires transfer of timing information between source and destination; maximum of 47-bytes of user data permitted in payload as an additional header byte is required to provide sequencing information.

AAL5 - **ATM Adaptation Layer** usually used for the transport of variable bit rate, delay-tolerant data traffic and signalling which requires little sequencing or error-detection support**.**

ANSI T1.630 - American National Standards Institute specification: Broadband ISDN - ATM Adaptation Layer for Constant Bit Rate Services Functionality and Specification.

Asynchronous - 1. Not **synchronous**; not periodic. 2. The temporal property of being sourced from independent timing references. Asynchronous signals have different frequencies, and no fixed phase relationship. 3. In telecom, data which is not synchronized to the public network clock. 4. The condition or state when an entity is unable to determine, prior to its occurrence, exactly when an event will transpire.

ATM - *Asynchronous Transfer Mod*e; a method in which information to be transferred is organized into fixed-length cells; asynchronous in the sense that the recurrence of cells containing information from an individual user is not necessarily periodic. (While ATM cells are transmitted synchronously to maintain clock between sender and receiver, the sender transmits data cells when it has something to send and transmits empty cells when idle, and is not limited to transmitting data every Nth cell.)

Cell - fixed-size information package consisting of 53 bytes (octets) of data; of these, 5 bytes represent the cell header and 48 bytes carry the user payload and required overhead.

CBR - *Constant Bit Rate*; an ATM service category supporting a constant or guaranteed rate, with timing control and strict performance parameters. Used for services such as voice, video, or circuit emulation.

CDV - *Cell Delay Variation*; a **QoS** parameter that measures the peak-to-peak cell delay through the network; results from buffering and cell scheduling.

CES - *Circuit Emulation Service*; ATM Forum service providing a virtual circuit which emulates the characteristics of a constant bit rate, dedicated-bandwidth circuit (e.g. T1).

CLP - *Cell Loss Priority*; a 1-bit field in the ATM cell header that corresponds to the loss priority of a cell; cells with CLP = 1 can be discarded in a congestion situation.

CSI - *Convergence Sublayer Indication* bit in the AAL1 header byte; when present in an even-numbered cell using **SDT**, indicates the presence of a pointer byte; used to transport **RTS** values in odd-numbered cells using **SRTS** for clock recovery.

GFC - *Generic Flow Control*; 4-bit field in the ATM header used for local functions (not carried end-to-end); default value is “0000”, meaning that GFC protocol is not enforced.

HEC - *Header Error Control*; using the fifth octet in the ATM cell header, ATM equipment (usually the **PHY**) may check for an error and correct the contents of the header; CRC algorithm allows for single-error correction and multiple-error detection.

I.363 - ITU-T Recommendation specifying the AALs for B-ISDN.

Isochronous - The temporal property of an event or signal recurring at known periodic time intervals (e.g. 125 µs). Isochronous signals are dependent on some uniform timing, or carry their own timing information embedded as part of the signal. Examples are DS-1/T1, E1 and TDM. From the root words, “iso” meaning equal, and “chronous” meaning time.

OAM bit - *Operations, Administration and Maintenance*; MSB within the **PTI** field of the ATM cell header which indicates if the ATM cell carries management information such as fault indications.

Plesiochronous - The temporal property of being arbitrarily close in frequency to some defined precision. Plesiochronous signals occur at nominally the same rate, any variation in rate being constrained within specific limits. Since they are not identical, over the long term they will be skewed from each other. This will force a

switch to occasionally repeat or delete data in order to handle buffer under-flow or overflow. (In telecommunications, this is known as a frame slip).

PHY - *Physical Layer*; bottom layer of the ATM Reference Model; provides ATM cell transmission over the physical interfaces that interconnect the various ATM devices.

PTI - *Payload Type Identifier*; 3-bit field in the ATM cell header - MSB indicates if the cell contains **OAM** information or user data; LSB indicates that a CBR-**AAL5** cell is the final cell in a frame.

QoS - *Quality of Service*; ATM performance parameters that characterize the transmission quality over a given VC (e.g cell delay variation; cell transfer delay, cell loss ratio).

RTS - *Residual Time Stamp*; see **SRTS.**

SAR - *Segmentation and Reassembly*; method of partitioning, at the source, frames into ATM cells and reassembling, at the destination, these cells back into information frames; lower sublayer of the **AAL** which inserts data from the information frames into cells and then adds the required header, trailer, and/or padding bytes to create 48-byte payloads to be transmitted to the ATM layer.

SDT - *Structured Data Transfer*; format used within **AAL1** for blocks consisting of N * 64 kbps channels; blocks are segmented into cells for transfer and additional overhead bytes (pointers) are used to indicate structure boundaries within cells (therefore aiding clock recovery).

SN - *Sequence Number*; 4-bit field in the **AAL1** header byte used as a sequence counter for detecting lost or misinserted ATM cells.

SNP - *Sequence Number Protection*; 4-bit field in the **AAL1** header byte consisting of a CRC and a parity bit which are designed to provide error-correction on the **SN.**

SRTS - *Synchronous Residual Time Stamp;* method for clock recovery in which difference signals between a source clock and the network reference clock (time stamps) are transmitted to allow reconstruction of the source clock. The destination reconstructs the source clock based on the time stamps and the network reference clock. (Note that the same network reference clock is required at both ends.)

SSRAM - *Synchronous Static RAM.*

Synchronous - 1. The temporal property of being sourced from the same timing reference. Synchronous signals have the same frequency, and a fixed (often implied to be zero) phase offset. 2. A mode of transmission in which the sending and receiving terminal equipment are operating continually at the same rate and are maintained in a desired phase relationship by an appropriate means.

UDT - *Unstructured Data Transfer*; format used within **AAL1** for transmission of user data without regard for structure boundaries (e.g. circuit emulation); term used within ANSI standard - not explicitly stated in ITU.

UTOPIA - *Universal Test and Operations Physical Interface for ATM;* a **PHY**-level interface to provide connectivity between ATM components.

VC - *Virtual Channel;* one of several logical connections defined within a virtual path (**VP**) between two ATM devices; provides sequential, unidirectional transport of ATM cells. Also *Virtual Circuit.*

VCI - *Virtual Channel Identifier;* 16-bit value in the ATM cell header that provides a unique identifier for the virtual channel (**VC**) within a virtual path (**VP**) that carries a particular cell.

VP - *Virtual Path;* a unidirectional logical connection between two ATM devices; consists of a set of virtual channels (**VC**).

VPI - *Virtual Path Identifier;* 8-bit value in the ATM cell header that indicates the virtual path (**VP**) to which a cell belongs.

VTOA - *Voice and Telephony over ATM;* intended to provide voice connectivity to the desktop, and to provide interoperability with existing N-ISDN and PBX services.

Glossary References:

The ATM Glossary - ATM Year 97 - Version 2.1, March 1997
The ATM Forum Glossary - May 1997
ATM and Networking Glossary (http://www.techguide.com/comm/index.html)
Mitel Semiconductor Glossary of Telecommunications Terms - May 1995.

2. Features

2.1 General

The MT90500 device external interfaces are:

- TDM (Time Division Multiplexed) bus composed of 16 serial streams running at up to 8.192 Mbps, plus related clocks and control signals, configurable by software. This interface also includes various signals for TDM clock signal generation. This bus carries telecom or other data in n x 64 kbps streams.
- Local serial TDM bus interface (a TDM input pin, a TDM output pin, and clocks).
- A primary UTOPIA bus running at up to 25 MHz, suitable for connection to a 25 Mbps or 155 Mbps PHY device.
- A secondary UTOPIA bus, for connection of an optional external SAR (e.g. data) device running at up to 25 MHz. In this case, the MT90500 device emulates a PHY device for the external SAR.
- A synchronous 36-bit wide memory interface running at up to 60 MHz.
- A 16-bit microprocessor interface used for device configuration, status, and control.
- Signals for general clocking, reset, and JTAG boundary-scan.

2.2 Serial TDM Bus

- Compatible with ST-BUS, MVIP, H-MVIP, IDL, and SCSA interfaces.
- Provides 16 bidirectional serial streams that can operate at TDM data rates of 2.048, 4.096 or 8.192 Mbps for up to 2048 TDM 64 kbps channels (1024 bidirectional DS0 channels).
- Serial TDM bus clocking schemes: TDM timing bus slave (MT90500 slaved to TDM bus), TDM timing bus master (MT90500 drives clocks onto TDM bus - freerun, or synchronized to 8 kHz reference) and TDM bus master-alternate (MT90500 slaved to TDM bus, but ready to switch to 8 kHz reference).
- Additional local TDM interface (2.048 Mbps) allows local TDM devices to access the main TDM bus.

2.3 CBR ATM Cell Processor

- Independent Segmentation and Reassembly blocks for receive and transmit (RX_SAR and TX_SAR) support CBR (Constant Bit Rate) transport of half- or full-duplex TDM channels.
- Compatible with “Structured Data Transfer (SDT) services” as per ANSI T1.630 standard for 1 to 122 TDM channels per VC.
- Compatible with ITU-T I.363.1 “circuit transport” of 8 kHz structured data using Structured Data Transfer (SDT) for 1 to 96 TDM channels per VC (using buffer-fill level monitoring).
- Compatible with ITU-T I.363.1 “voiceband signal transport.”
- Compatible with AF-VTOA-0078.000 “N x 64 Basic Service” (non-CAS) Circuit Emulation (using buffer-level monitoring, rather than lost cell insertion).
- Compatible with AF-VTOA-0078.000 for SDT of partially-filled AAL1 cells with N-channel structures (where N does not exceed the value of the partial-fill).
- AAL1 SAR-PDU Header processing (AAL1 Sequence Number checking).
- Supports up to 1024 bidirectional VCs (virtual circuits) simultaneously.
- Supports up to 1024 transmit TDM channels and 1024 receive TDM channels simultaneously.
- Supports CBR-AAL0 (48 byte cell payload).
- Supports CBR-AAL5 as per AF-VTOA-0083.000, also supports nx64 trunking over CBR-AAL5.
- Supports partially-filled cells (AAL1, CBR-AAL5, and CBR-AAL0).

- User-defined, per-VC, Cell Delay Variation tolerance: 8 to 128 ms buffer size (up to 64 ms CDV).
- Handles TDM channels at 64 kbps granularity.
- Each individual VC can be composed of n x 64 kbps wideband channels (n = 1, 2, ..., 122).
- Flexible aggregation capabilities (n x 64 kbps) maintain frame integrity, while allowing any combination of 64 kbps channels (DS0 grooming).
- A VC can contain any combination of TDM channels from any combination of TDM streams (n x 64) and maintain frame integrity for those channels.
- Supports several 8 kHz synchronisation operations: synchronized to external 8 kHz reference, synchronized to network clock, and synchronized to timing derived from an ATM VC (including ITU-T I.363.1 Adaptive clock recovery mechanism).

2.4 External Memory Interface

- To implement SAR functions and buffers, the MT90500 device uses external Synchronous SRAM.
- External Synchronous SRAM size is chosen by user, and depends on Cell Delay Variation (CDV) and the number of simultaneous 64 kbps channels handled. The amount of Synchronous SRAM is scalable to suit the application, and may range from 128 Kbytes to 2,048 Kbytes.

2.5 UTOPIA Interface and Multiplexer

- UTOPIA Level 1 compatible 8-bit bus, running at up to 25 Mbyte/s, for connection to PHY devices with data throughput of up to 155 Mbps.
- Transmit multiplexer mixes cells from TX_SAR and Secondary UTOPIA port, supporting another MT90500, and/or an external SAR device (e.g. AAL5) connected to a single PHY device.
- Programmable multiplexer priority gives internally generated AAL1 cells equal, or higher, priority than cells coming from Secondary UTOPIA port.
- Supports non-CBR data cells and OAM cells destined for microprocessor with Receive and Transmit Data Cell FIFOs.
- Flexible receive cell handling: AAL1 (as well as CBR-AAL0 and CBR-AAL5) cells are sent to the TDM port; data cells (non-CBR data and OAM cells) are sent to the Receive Data Cell FIFO; cells with unrecognized VCs may be queued or ignored.
- Cell reception based on look-up-table allows flexible VC assignment for CBR VCs (allows non-contiguous VC assignment).
- Programmable VPI/VCI Match and Mask filtering reduces unnecessary look-up-table accesses.

2.6 Microprocessor Interface

- 16-bit microprocessor port, configurable to Motorola or Intel timing.
- Programmable interrupts for control and statistics.
- Allows access to internal registers for initialization, control, and statistics.
- Allows access to external SSRAM for initialization, control, and observation.

2.7 Miscellaneous

- Master clock rate up to 60 MHz.
- Dual rails (3.3V for power minimization, 5V for standard I/O).
- Loopback function provided at the TDM interface.
- IEEE 1149 (JTAG) Boundary-Scan Test Access Port for testing board-level interconnect.
- Packaging: 240-pin PQFP.

2.8 Interrupts

The MT90500 provides a wide variety of interrupt source bits, allowing for easy monitoring of MT90500 operation. All interrupt source bits, including the module level interrupt bits, have an associated mask bit which enables or disables assertion of the interrupt pin. This enables the user to tailor the interrupt pin activity to the application. Interrupt source bits are set regardless of the state of the associated mask bit, so even source bits which are disabled from causing an interrupt pin assertion may be polled by the CPU by reading the appropriate register.

2.8.1 Module Level Interrupts

The following interrupt bits are used to indicate which MT90500 circuit module is the source of the interrupt. They are set when one or more interrupt source bits in the particular circuit module is set. The CPU can find the source of an interrupt by reading the register containing these bits and then reading the indicated module's interrupt register.

- TX_SAR Module Interrupt
- RX_SAR Module Interrupt
- UTOPIA Module Interrupt
- TDM Module Interrupt
- Timing (TDM Clock Generation) Module Interrupt

2.8.2 TX_SAR Interrupts

- Transmit Non-CBR Data Cell FIFO Overrun Interrupt
- Scheduler error (Indicates that the TX_SAR has too heavy a work load.)

2.8.3 RX_SAR Interrupts

- AAL1-byte Parity Error Interrupt
- AAL1-byte CRC Error Interrupt
- AAL1-byte Sequence Number Error Interrupt
- Pointer-byte Parity Error Interrupt
- Pointer-byte Out of Range Error Interrupt
- Underrun Error Interrupt
- Overrun Error Interrupt
- Misc. Counter Rollover Interrupt
- Underrun Counter Rollover Interrupt
- Overrun Counter Rollover Interrupt

2.8.4 UTOPIA Interrupts

- Receive Non-CBR Data Cell FIFO Overrun Interrupt
- RX UTOPIA Module Internal FIFO Overrun Interrupt
- Receive Non-CBR Data Cell FIFO Receive Cell Interrupt

2.8.5 TDM Interrupts

- Clock Absent Interrupt
- Clock Fail Interrupt
- TDM Out of Bandwidth Interrupt
- TDM Read Underrun Error Interrupt
- TDM Read Underrun Counter Rollover Interrupt

2.8.6 Timing Module Interrupts

- 8 kHz Reference Failure Interrupt
- Adaptive Clock Loss of Timing Reference Cell Interrupt
- Adaptive Clock Loss of Synchronization Interrupt

2.9 Statistics

The MT90500 provides a number of statistics to allow monitoring of the MT90500. These statistics generally parallel the operation of some of the interrupt source bits. The counters (except the Timing Recovery counters) also set rollover interrupt source bits when they reach their terminal counts and return to zero.

2.9.1 RX_SAR Statistics

- Misc. Event Counter: This 16-bit register's value is incremented each time a (mask-selected) miscellaneous error occurs.
  - AAL1-byte Parity Error
  - AAL1-byte CRC Error
  - AAL1 Sequence Number Error
  - Pointer-byte Parity Error
  - Pointer-byte Out of Range Error
- Misc. Event ID Register: The address of the RX Control Structure that caused the last miscellaneous error.
- Underrun Count: This 16-bit register's value is incremented each time a CBR Receive Underrun occurs.
- Underrun ID Number: The address of the RX Control Structure that caused the last underrun error.
- Overrun Count: This 16-bit register is incremented each time a CBR Receive Overrun occurs.
- Overrun ID Number: The address of the RX Control Structure that caused the last overrun error.

2.9.2 TDM Statistics

- TDM Read Underrun Time Slot Stream. Contains the time slot and stream on which the last TDM read underrun was detected.
- TDM Read Underrun Counter. Each time a TDM read underrun occurs, this register's value is incremented.

2.9.3 Timing Recovery Statistics

- Event Counter: Counts the reception of timing reference cells or 8 kHz markers.
- CLKx1 Counter: 24-bit counter which keeps a running count of TDM byte-periods.

3. Pin Descriptions

I/O types are: Output (O), Input (I), Bidirectional (I/O), Power (PWR), or Ground (GND).

Input pad types are: TTL, CMOS, Differential, or Schmitt. The notations “PU” and “PD” are used, respectively, to indicate that a pad has an internal pullup or pulldown resistor. TTL (5V) inputs are pulled-up to the 5V rail, CMOS (3.3V) inputs are pulled-up to the 3.3V rail. These weak internal resistors should not be relied upon for fast data transitions. The 3.3V CMOS inputs have a switching threshold of 1.6V, and tolerate input levels of up to 5V; therefore they are 5V TTL compatible (with the exception of the $\overline{\text{TRISTATE}}$ pin, which is not 5V tolerant).

Output pad types are generally described by voltage and current capability. Output types used are: 3.3V, 4mA; 5V, 4mA; 5V, 12mA; and open-drain. A notation of “SR” indicates that the pad is slew-rate limited. 3.3V CMOS outputs will satisfy 5V TTL input thresholds at the rated current.

Table 1 - Primary UTOPIA Bus Pins

Pin #	Pin Name	I/O	Type	Description
49, 48, 47, 46, 45, 44, 39, 38	PTXDATA[7:0]	O	5V, 4mA	Primary UTOPIA transmit data bus. Byte-wide data driven from MT90500 to PHY device. Bit 7 is the MSB.
52	PTXSOC	O	5V, 4mA	Primary UTOPIA transmit start of cell signal. Asserted by the MT90500 when PTXDATA[7:0] contains the first valid byte of the cell.
51	$\overline{\text{PTXEN}}$	O	5V, 4mA	Primary UTOPIA transmit data enable. Active LOW signal asserted by the MT90500 during cycles when PTXDATA[7:0] contains valid cell data.
53	PTXCLAV	I	TTL PU	Primary UTOPIA transmit cell available indication signal. For cell level flow control, PTXCLAV is asserted by the PHY to indicate to the MT90500 that the PHY can accept the transfer of a complete cell.
82	PTXCLK	I/O	TTL PU / 5V, 4mA SR	Primary UTOPIA transmit clock. Data transfer & synchronization clock provided by the MT90500 to the PHY for transmitting data on PTXDATA[7:0]; software configurable (in Main Control Register at 0000h) to run at up to 25 MHz. Note that this pin should be configured as an output for exact compliance with UTOPIA Level 1, V2.01.
50	PTXPAR	O	5V, 4mA	Primary UTOPIA transmit parity. This signal is the odd parity bit over PTXDATA[7:0].
57, 58, 59, 62, 63, 64, 65, 66	PRXDATA[7:0]	I	TTL PU	Primary UTOPIA receive data bus. Byte-wide data driven from the PHY to the MT90500. PRXDATA[7] is the MSB.
56	PRXSOC	I	TTL PU	Primary UTOPIA receive start of cell signal. Asserted by the PHY when PRXDATA[7:0] contains the first valid byte of a cell.
55	$\overline{\text{PRXEN}}$	I	TTL PU	Primary UTOPIA bus data enable. Active LOW signal normally asserted by the secondary SAR to indicate that PRXDATA[7:0], PRXSOC, and PRXCLAV will be sampled at the end of the next clock cycle. If no secondary SAR is used, ground this pin at the MT90500 and PHY devices. Note that the UTOPIA standard permits this signal to be permanently asserted (see UTOPIA Level 1, V2.01, footnote 6).
54	PRXCLAV	I	TTL PU	Primary UTOPIA receive cell available indication signal. For cell level flow control, PRXCLAV is asserted by the PHY to indicate it has a complete cell available for transfer to the RX UTOPIA port.
79	PRXCLK	I	TTL PU	Primary UTOPIA bus receive clock. This clock, which can run at up to 25 MHz, is provided by the secondary SAR device. If no secondary SAR is used, connect to PTXCLK (this will provide exact compliance with the UTOPIA Level 1, V2.01 specification).

Refer to Figure 58 on page 125 for implementation details regarding the interface between two MT90500s and an external AAL5 SAR.

Table 2 - Secondary UTOPIA Bus Pins

Pin #	Pin Name	I/O	Type	Description
70, 71, 72, 73, 74, 75, 76, 77	STXDATA[7:0]	I	TTL PU	Secondary UTOPIA transmit data bus. Byte-wide data driven from the external SAR to the MT90500. Bit 7 is the MSB.
69	STXSOC	I	TTL PU	Secondary UTOPIA transmit start of cell signal. Asserted by the external SAR device when STXDATA[7:0] contains the first valid byte of the cell.
68	$\overline{\text{STXEN}}$	I	TTL PU	Secondary UTOPIA transmit data enable. Active LOW signal asserted by the external SAR during cycles when STXDATA[7:0] contains valid cell data.
67	STXCLAV	O	5V, 4mA	Secondary UTOPIA transmit cell available indication signal. For cell level flow control, STXCLAV is asserted by the MT90500 to indicate to the external SAR that the MT90500 can accept the transfer of a complete cell.
85	STXCLK	I	TTL PU	Secondary UTOPIA transmit clock, which can run at up to 25 MHz. Data transfer & synchronization clock provided by the external SAR to the MT90500 for transmitting data over STXDATA[7:0].

Note: MT90500 Secondary UTOPIA port emulates a PHY device for connection to an external SAR (ATM-layer device).
Refer to Figure 58 on page 125 for implementation details regarding the interface between two MT90500s and an external AAL5 SAR.

Table 3 - Microprocessor Bus Interface Pins

Pin #	Pin Name	I/O	Type	Description
37	Intel/$\overline{\text{Motorola}}$	I	TTL PU	Intel interface (1) / Motorola interface (0)
36	IC	I	TTL PU	Internal connection (must be HIGH).
203	$\overline{\text{CS}}$	I	TTL PU	Active LOW chip select signal.
237	$\overline{\text{WR}}$/R\$\overline{\text{W}}$	I	TTL PU	Active LOW Write Strobe (Intel) / Read_$\overline{\text{Write}}$ (Motorola).
239	$\overline{\text{RD}}$/$\overline{\text{DS}}$	I	TTL PU	Active LOW Read Strobe (Intel) / Active LOW Data Strobe (Motorola).
238	RDY/$\overline{\text{DTACK}}$	O	5V, 4mA	Ready (Intel) / Active LOW Data Transfer Acknowledge (Motorola). Acts as pseudo-open-drain in Motorola mode ($\overline{\text{DTACK}}$).
84	$\overline{\text{INT}}$	O	5V, 4mA SR (Open-Drain)	Active LOW interrupt line.
223, 222, 219, 218, 217, 216, 215, 214, 212, 211, 210, 209, 208, 206, 205, 204	D[15:0]	I/O	TTL PU / 5V, 4mA SR	CPU data bus.
184	AEM	I	TTL PU	Access External Memory - CPU accesses external memory when HIGH (internal memory and registers when LOW).
185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 198, 199, 202	A[15:1]	I	TTL PU	CPU Address lines A15-A1. All microprocessor accesses to the device are word-wide, but addresses in this document are given as byte-addresses. The virtual A[0] bit selects between high and low bytes in a word.

Table 4 - External Memory Interface Pins

Pin #	Pin Name	I/O	Type	Description
98	MEMCLK	O	3.3V, 4mA	Memory Clock. Internally connected to MCLK.
147	$\overline{\text{MEM\_CS0L}}$	O	3.3V, 4mA	Active LOW memory chip select signal. This chip select is used in all memory modes. When there are two chips per bank, $\overline{\text{MEM\_CS0L}}$ is associated with MEM_DAT[15:0] of Bank 0.
176	$\overline{\text{MEM\_CS0H}}$	O	3.3V, 4mA	Active LOW memory chip select signal. This chip select is used when there are two 16-bit memory chips per bank. $\overline{\text{MEM\_CS0H}}$ is associated with MEM_DAT[31:16] of Bank 0.
148	$\overline{\text{MEM\_CS1L}}$	O	3.3V, 4mA	Active LOW memory chip select signal. This chip select is used when there are two banks and two chips per bank. $\overline{\text{MEM\_CS1L}}$ is associated with MEM_DAT[15:0] of Bank 1.
177	$\overline{\text{MEM\_CS1H}}$	O	3.3V, 4mA	Active LOW memory chip select signal. This chip select is used when there are two banks and two chips per bank. $\overline{\text{MEM\_CS1H}}$ is associated with MEM_DAT[31:16] of Bank 1.
178, 179, 149, 150	$\overline{\text{MEM\_WR[3:0]}}$	O	3.3V, 4mA	Active LOW byte-write enables. $\overline{\text{MEM\_WR[3]}}$ is associated with MEM_DAT[31:24]; $\overline{\text{MEM\_WR[2]}}$ is associated with MEM_DAT[23:16]; $\overline{\text{MEM\_WR[1]}}$ is associated with MEM_DAT[15:8]; $\overline{\text{MEM\_WR[0]}}$ is associated with MEM_DAT[7:0].
180	$\overline{\text{MEM\_OE}}$	O	3.3V, 4mA	Active LOW output enable.
123, 122, 121, 118, 117, 116, 115, 103, 102, 99, 146, 144, 130, 128, 127, 126, 125, 124	MEM_ADD[17:0]	O	3.3V, 4mA	Memory address lines.
166, 167, 168, 170, 171, 173, 174, 175, 153, 154, 155, 156, 158, 159, 162, 164, 133, 134, 135, 136, 137, 138, 142, 143, 105, 106, 107, 108, 109, 112, 113, 114	MEM_DAT[31:0]	I/O	3.3V CMOS PU / 3.3V 4mA	Memory data lines. MEM_DAT[31:24] represent the upper byte; MEM_DAT[23:16] represent the upper-middle byte; MEM_DAT[15:8] represent the lower-middle byte; MEM_DAT[7:0] represent the lower byte.
165, 152, 131, 104	MEM_PAR[3:0]	I/O	3.3V CMOS PU / 3.3V 4mA	Memory parity lines. MEM_PAR[3:0] are the optional “parity” bits that allow TDM Read Underrun detection. MEM_PAR[3] is related to MEM_DAT[31:24], MEM_PAR[2] is related to MEM_DAT[23:16], MEM_PAR[1] is related to MEM_DAT[15:8], and MEM_PAR[0] is related to MEM_DAT[7:0]. When unused, these pins must be pulled up via external resistors.

Table 5 - Master Clock, Test, and Power Pins

Pin #	Pin Name	I/O	Type	Description
87	MCLK	I	TTL PU	Master Clock. This signal drives the internal logic (including the RX_SAR and the TX_SAR) and the external memory (through MEMCLK). 60 MHz for most applications. MCLK should be more than 5 times CLKx1.
78	$\overline{\text{RESET}}$	I	5V TTL Schmitt PU	Chip reset signal (active LOW). Note that the MT90500 is synchronously reset, and that MCLK should be applied during reset. To asynchronously tristate outputs, assert the $\overline{\text{TRISTATE}}$ pin. The $\overline{\text{TRST}}$ pin (JTAG reset) should also be asserted LOW during chip reset. Reset should last at least 2 µs when MCLK is 60 MHz. Also see $\overline{\text{SRES}}$ bit in register 0000h.
97	TMS	I	3.3V CMOS PU	JTAG Test Mode Select signal.
93	TCK	I	3.3V CMOS PU	JTAG Test Clock.
95	TDI	I	3.3V CMOS PU	JTAG Test Data In.
96	TDO	O	3.3V, 4mA SR	JTAG Test Data Out. **Note:** TDO is tristated by $\overline{\text{TRISTATE}}$ pin.
94	$\overline{\text{TRST}}$	I	3.3V CMOS PD	JTAG Test Reset input (active LOW). Should be asserted LOW on power-up and during reset. Must be HIGH for JTAG boundary-scan operation. **Note:** This pin has an internal **pull-down**.
1, 7, 16, 29, 43, 61, 86, 91, 110, 119, 129, 139, 151, 163, 172, 182, 197, 213, 229	IO_VSS	GND		Ground for I/O logic.
100, 141, 161	CORE_VSS	GND		Ground for core logic.
20, 40, 80, 201, 221	RING_VSS	GND		Ground for core logic.
92, 111, 120, 132, 145, 157, 169, 181	IO_VDD_3V	PWR		Power for I/O logic (3.3 V).
2, 13, 24, 42, 60, 88, 183, 207, 225, 240	IO_VDD_5V	PWR		Power for I/O logic (5 V).
101, 140, 160	CORE_VDD_3V	PWR		Power for core logic (3.3 V).
21, 41, 81, 200, 220	RING_VDD_3V	PWR		Power for core logic (3.3 V).
89	IC	I		IC TEST, must be grounded.
90	$\overline{\text{TRISTATE}}$	I	3.3V CMOS PU **3.3V ONLY**	Output Tristate Control. Asynchronously tristates all output pins when LOW. Can be asserted LOW on power-up and during reset. Pull up to 3.3V for normal operation. **NOT 5V TOLERANT.**

Table 6 - TDM Port Pins

Pin #	Pin Name	I/O	Type	Description
25, 23, 22, 19, 18, 17, 15, 14, 12, 11, 10, 9, 8, 6, 5, 4	ST[15:0]	I/O	TTL PU / 5V, 12mA SR	TDM data streams. Used to pass PCM (voice) bytes or other data types. For PCM bytes, the first bit is the sign bit. In order to enable any of these pins as outputs, the GENOE bit in the TDM Interface Control Register (6000h) must be set, as well as the appropriate channel bits in the Output Enable Registers.
230	CLKx2PI	I	Diff +	Differential clock signal input (+) running at twice the serial TDM data stream frequency. This pin is used only in differential clock mode (H-MVIP) and should be tied HIGH when not in use. For normal (non-differential) clock mode input, use CLKx2/CLX2PO pin.
227	CLKx2NI	I	Diff -	Differential clock signal input (-) running at twice the serial TDM data stream frequency. This pin is used only in differential clock mode (H-MVIP) and should be grounded when not in use.
233	CLKx1	I/O	TTL PU / 5V, 12mA SR	Clockx1. This signal represents the CLKx2 signal divided by 2.
232	FSYNC	I/O	TTL PU / 5V, 12mA SR	Frame sync. Bidirectional 8 kHz reference to/from main TDM Bus.
30	IC	I	TTL PU	Internal connection (must be HIGH).
32	CORSIGA / CLKFAIL	I/O	TTL PU / 5V, 12mA SR	CORSIGA I/O when not used by the TDM bus. Clock fail on SCSA bus.
235	CORSIGB / MC	I/O	TTL PU / 5V, 12mA SR	CORSIGB I/O when not used by the TDM bus. Message Channel (I/O) on the SCSA bus.
33	CORSIGC / MCTX	I/O	TTL PU / 5V, 4mA SR	CORSIGC I/O when not used by the TDM bus. Message Channel Transmit (input) toward SCSA bus from HDLC controller.
34	CORSIGD / MCRX	I/O	TTL PU / 5V, 4mA SR	CORSIGD I/O when not used by the TDM bus. Message Channel Receive (output) from SCSA bus toward HDLC controller.
35	CORSIGE / MCCLK	I/O	TTL PU / 5V, 4mA SR	CORSIGE I/O when not used by the TDM bus. Message Channel HDLC controller clock (output) from the SCSA bus.
83	EX_8KA	I	TTL PU	An 8 kHz clock input that can be used as reference in the generation of the REF8KCLK or SEC8K lines.
234	SEC8K	I/O	TTL PU / 5V, 12mA	Secondary alternate 8 kHz clock. Compatible with MVIP and H-MVIP modes.
226	REF8KCLK	O	5V, 12mA SR	An 8 kHz clock generated internally. This signal is generated from one of several internal sources which are programmed by the user. This output can provide a reference clock to an external PLL to generate the 16.384 / 32.768 MHz required for the operation of the IC in master mode.
224	PLLCLK	I	TTL PU	16.384 / 32.768 MHz TDM clock reference from external PLL.
31	FREERUN	O	5V, 12mA SR	Active HIGH external PLL freerun indication.
236	LOCx2	O	5V, 4mA SR	Local TDM Bus Clockx2.
3	LOCx1	O	5V, 4mA SR	Local TDM Bus Clockx1.
28	LSYNC	O	5V, 4mA SR	Local TDM Bus Frame Sync.
26	LOCSTo	O	5V, 4mA SR	Local TDM Bus Serial Data Out Stream.
27	LOCSTi	I	TTL PU	Local TDM Bus Serial Data In Stream.
231	CLKx2/CLKx2PO	I/O	TTL PU / 5V, 12mA	CLKx2 Input/Output / CLKx2 Positive Output. Normal (non-differential) CLKx2 input in TDM Clock Slave mode. CLKx2 output (differential and non-differential) in TDM Clock Master mode.
228	CLKx2NO	O	5V, 12mA	CLKx2 Negative Output. Differential negative output clock. (Inverse of CLKx2PO). Used in TDM Clock Master, differential clock mode (H-MVIP); active whenever MT90500 is TDM Clock Master. (Leave unconnected if non-differential clock desired.)

Table 7 - Reset State of I/O and Output Pins

Pin Name	I/O	Reset State	Additional Control Information
PTXDATA[7:0]	O	Active during and after reset.	N / A
PTXPAR	O	Active during and after reset.	N / A
PTXCLK	I/O	High-impedance	The PTXCLK_SEL bits in the Main Control Register (0000h) are LOW after reset; PTXCLK is tristated and an input.
$\overline{\text{PTXEN}}$	O	Active during and after reset.	N / A
PTXSOC	O	Active during and after reset.	N / A
STXCLAV	O	Active during and after reset.	N / A
MEMCLK	O	Continues to drive at MCLK rate during reset.	N / A
$\overline{\text{MEM\_CS[1:0][H:L]}}$	O	Active during and after reset.	N / A
$\overline{\text{MEM\_WR[3:0]}}$	O	Active during and after reset.	N / A
$\overline{\text{MEM\_OE}}$	O	Active HIGH during reset.	$\overline{\text{RESET}}$ LOW forces this pin HIGH. After reset, this pin goes LOW.
MEM_ADD[17:0]	O	Active during and after reset.	N / A
MEM_DAT[31:0]	I/O	High-impedance	N / A
MEM_PAR[3:0]	I/O	High-impedance	N / A
RDY/$\overline{\text{DTACK}}$	O	Active during and after reset. **Tristated when $\overline{\text{CS}}$ is HIGH.**	In Motorola mode, pin drives HIGH during reset. In Intel mode, drives LOW during reset.
$\overline{\text{INT}}$	O	High-impedance	The interrupt enable bits in the Main Control Register at 0000h are reset to zero; interrupts are masked after reset.
D[15:0]	I/O	High-impedance	N / A
TDO	O	Determined by $\overline{\text{TRST}}$ and / or TAP controller state	N / A
ST[15:0]	I/O	High-impedance	The GENOE bit in the TDM Interface Control Register (6000h) is LOW after reset; these TDM data pins are tristated and in loopback mode.
CLKx1	I/O	Input	The CLKMASTER bit in the TDM Bus Type Register (6010h) resets to ‘0’; the MT90500 is TDM Slave, and CLKx1 is input from the TDM bus.
FSYNC	I/O	Input	The CLKMASTER bit in the TDM Bus Type Register (6010h) resets to ‘0’; the MT90500 is TDM Slave and FSYNC is input from the TDM bus.
CORSIGA/ CLKFAIL	I/O	Input	The TDM I/O Register at 6004h resets to all zeroes; all CORSIGxCNF are set to “00” and all CORSIGx pins are configured as inputs.
CORSIGB / MC	I/O	Input	See CORSIGA.
CORSIGC / MCTX	I/O	Input	See CORSIGA.
CORSIGD / MCRX	I/O	Input	See CORSIGA.
CORSIGE / MCCLK	I/O	Input	See CORSIGA.
SEC8K	I/O	Input	The SEC8KEN bit in the Master Clock Generation Control Register (6090h) resets to ‘0’; SEC8K is an input.
REF8KCLK	O	Active during and after reset.	Due to the reset values of the Master Clock Generation Control Register (6090h) and the Master Clock / CLKx2 Division Factor (6092h), REF8KCLK is initially equal to MCLK / 8194.
FREERUN	O	Active HIGH during and after reset.	The FREERUN bits in the Master Clock Generation Control Register at 6090h are “00” after reset; the FREERUN pin is reset to active HIGH.
LOCx2	O	Active during and after reset.	N / A
LOCx1	O	Active during and after reset.	N / A
LSYNC	O	Active during and after reset.	N / A
LOCSTo	O	Active during and after reset.	N / A

Table 7 - Reset State of I/O and Output Pins

Pin Name	I/O	Reset State	Additional Control Information
CLKx2/CLKx2PO	I/O	Input	The CLKMASTER bit in the TDM Bus Type Register (6010h) resets to '0'; the MT90500 is TDM Slave and CLKx2 is input from the TDM bus.
CLKx2NO	O	High-impedance	The CLKMASTER bit in the TDM Bus Type Register (6010h) resets to '0'; the MT90500 is TDM Slave and therefore no clock signals are driven from the MT90500.
Note: All pins are placed in high-impedance by asserting the $\overline{\text{TRISTATE}}$ pin.			

Table 8 - Pinout Summary

Type	Input	Output	I/O	Power	Ground
Primary UTOPIA	13	11	1		
Secondary UTOPIA	11	1			
External Memory Interface		28	36		
Microprocessor Interface	21	2	16		
Miscellaneous	8	1			
TDM Interface	6	7	25		
Power				26	
Ground					27
Total 187 + 26 + 27 = 240	**59**	**50**	**78**	**26**	**27**

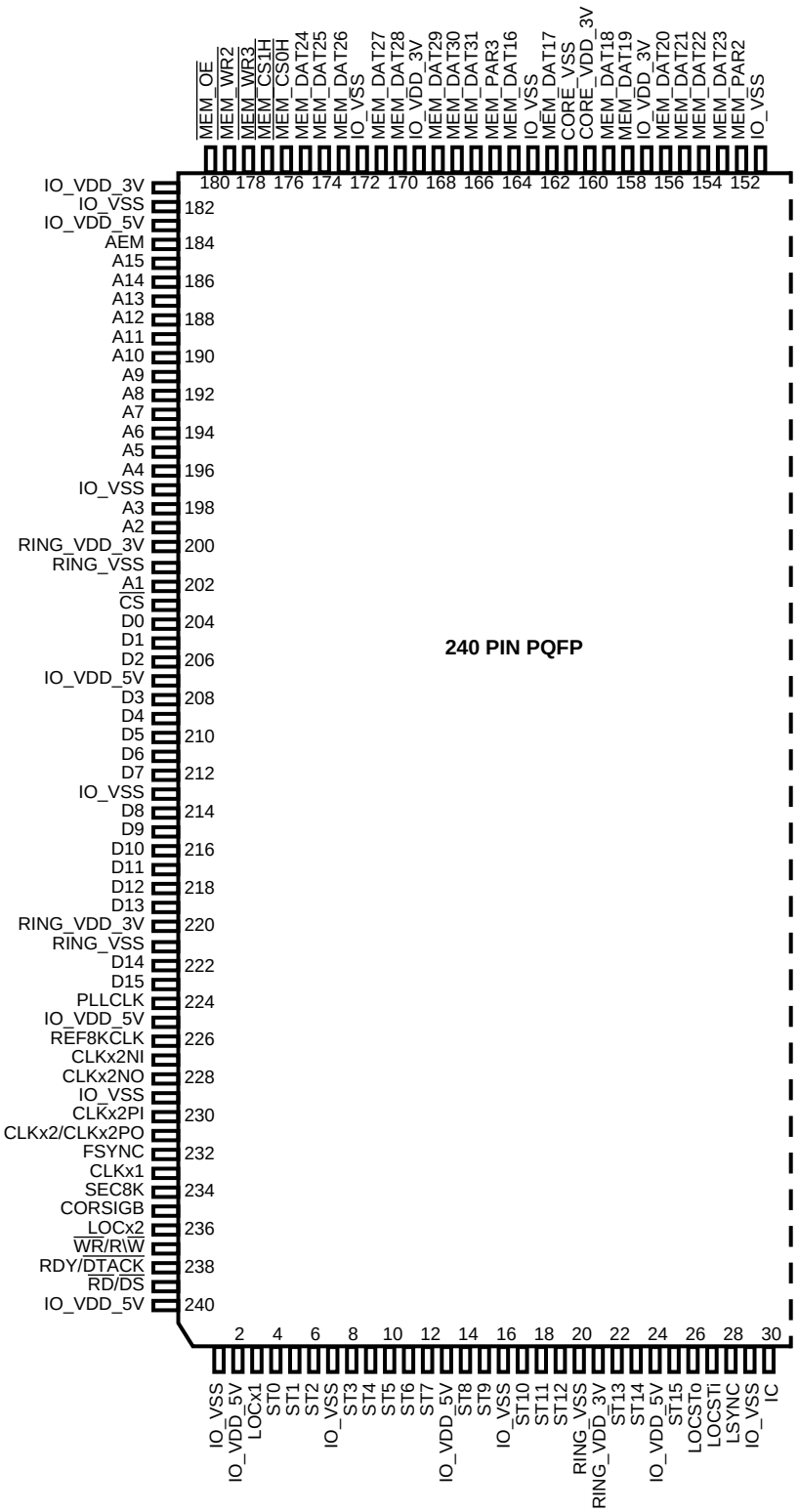
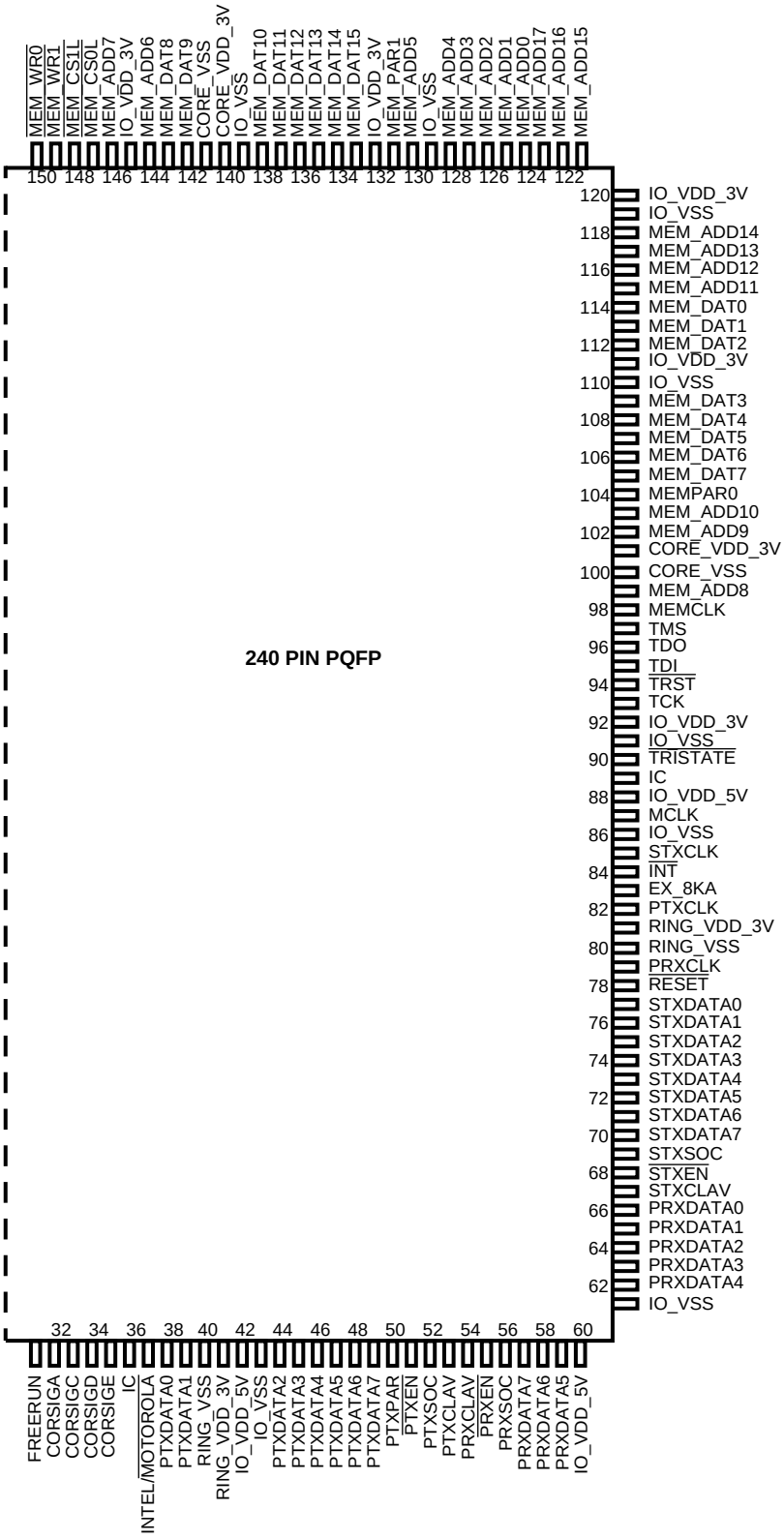


Figure 2. Pin Connections


240 PIN PQFP
MEM_WR0
MEM_WR1
MEM_CS1L
MEM_CS0L
MEM_ADD7
IO_VDD_3V
MEM_ADD6
MEM_DAT8
MEM_DAT9
CORE_VSS
CORE_VDD_3V
IO_VSS
MEM_DAT10
MEM_DAT11
MEM_DAT12
MEM_DAT13
MEM_DAT14
MEM_DAT15
IO_VDD_3V
MEM_PAR1
MEM_ADD5
IO_VSS
MEM_ADD4
MEM_ADD3
MEM_ADD2
MEM_ADD1
MEM_ADD0
MEM_ADD17
MEM_ADD16
MEM_ADD15
150 148 146 144 142 140 138 136 134 132 130 128 126 124 122
120 IO_VDD_3V
IO_VSS
118 MEM_ADD14
MEM_ADD13
116 MEM_ADD12
MEM_ADD11
114 MEM_DAT0
MEM_DAT1
112 MEM_DAT2
IO_VDD_3V
110 IO_VSS
MEM_DAT3
108 MEM_DAT4
MEM_DAT5
106 MEM_DAT6
MEM_DAT7
104 MEMPAR0
MEM_ADD10
102 MEM_ADD9
CORE_VDD_3V
100 CORE_VSS
MEM_ADD8
98 MEMCLK
TMS
96 TDO
TDI
94 TRST
TCK
92 IO_VDD_3V
IO_VSS
90 TRISTATE
IC
88 IO_VDD_5V
MCLK
86 IO_VSS
STXCLK
84 INT
EX_8KA
82 PTXCLK
RING_VDD_3V
80 RING_VSS
PRXCLK
78 RESET
STXDATA0
76 STXDATA1
STXDATA2
74 STXDATA3
STXDATA4
72 STXDATA5
STXDATA6
70 STXDATA7
STXSOC
68 STXEN
STXCLAV
66 PRXDATA0
PRXDATA1
64 PRXDATA2
PRXDATA3
62 PRXDATA4
IO_VSS
32 34 36 38 40 42 44 46 48 50 52 54 56 58 60
FREERUN
CORSIGA
CORSIGC
CORSIGD
CORSIGE
IC
INTEL/MOTOROLA
PTXDATA0
PTXDATA1
RING_VSS
RING_VDD_3V
IO_VDD_5V
IO_VSS
PTXDATA2
PTXDATA3
PTXDATA4
PTXDATA5
PTXDATA6
PTXDATA7
PTXPAR
PTXEN
PTXSOC
PTXCLAV
PRXCLAV
PRXEN
PRXSOC
PRXDATA7
PRXDATA6
PRXDATA5
IO_VDD_5V

4. Functional Description

As shown in Figure 1, “MT90500 Block Diagram,” on page 10, the MT90500 device consists of the following major components: TDM Module, External Memory Controller, TX_SAR, RX_SAR, UTOPIA Module, Clock Recovery, Microprocessor Interface, and Test Interface. This section describes each module in detail.

4.1 TDM Module

This circuit module is the interface to the Time Division Multiplexed (TDM) buses, which carry N x 64kbps data. The TDM module interfaces are:

- 16 bidirectional TDM data streams on pins ST[15:0]; these pins can be configured through software registers to support various bus formats (ST-BUS, MVIP, H-MVIP, SCSA, or IDL) and data rates of 2.048 Mbps, 4.096 Mbps, or 8.192 Mbps; (For the selection of the bus type, see TDM Bus Type Register at address 6010h in Section 5.)
- the TDM bus clocks (CLKx2, CLKx1) and frame synchronization signal (FSYNC);
- the TDM bus ancillary signals such as SEC8K (MVIP) and CLKFAIL (SCSA);
- a local TDM bus (LOCx2, LOCx1, LSYNC, LOCSTi, and LOCSTo); the format of the bus, which runs at 2.048 Mbps (LOCx2 = 4.096 Mbps), is user-selectable via software (see Local Bus Type Register at address 6020h).

The TDM module moves TDM data from the TDM serial inputs to the external memory (where it is read by the TX_SAR) in the transmit direction, and from the external memory (where it was written by the RX_SAR) to the TDM outputs in the receive direction. This is done with the aid of an internal TDM frame buffer, which is used to buffer 4 frames of each TDM channel in both directions; i.e. four frames in the receive direction (ATM to TDM), and four frames in the transmit direction (TDM to ATM). The TDM module can be divided into four main processes:

- TDM Clock Logic, which controls all the operations related to clock generation and clock signal monitoring on the TDM bus;
- TDM Interface Operation, which controls the input and output of the serial TDM data;
- TDM Data to External Memory Process, which transfers TDM input data into Transmit Circular Buffers in the external memory;
- External Memory to TDM Data Output Process, which transfers TDM output data from Receive Circular Buffers in the external memory to the TDM output bus.

Each of these processes are described in detail below.

4.1.1 TDM Clock Logic

The TDM Clock Logic controls all of the operations related to clock generation and clock signal monitoring on the TDM bus. The block diagram of the TDM Clock Logic is shown in Figure 3. This module consists of several blocks, including: selection logic for an 8 kHz reference for the external PLL (REF8KCLK), the main TDM bus clock generation logic, the local TDM bus clock generation logic, the clock drivers & clock selection for the SEC8K signal, and the clock failure detection logic.

4.1.1.1 TDM Timing Modes

The MT90500 supports 4 major TDM timing modes. There are also a number of TDM timing features which are independent of the TDM timing mode being used:

- The SEC8K pin (MVIP compatibility) can be programmed as either output or input. The SEC8KEN bit in the MCGCR Register (6090h) enables the SEC8K pin driver. If the SEC8K pin is enabled as an output, the SEC8KSEL bit in the same register selects the source for this signal (the EX_8KA input, or the internal 8 kHz FS_INT signal which is derived from CLK16).

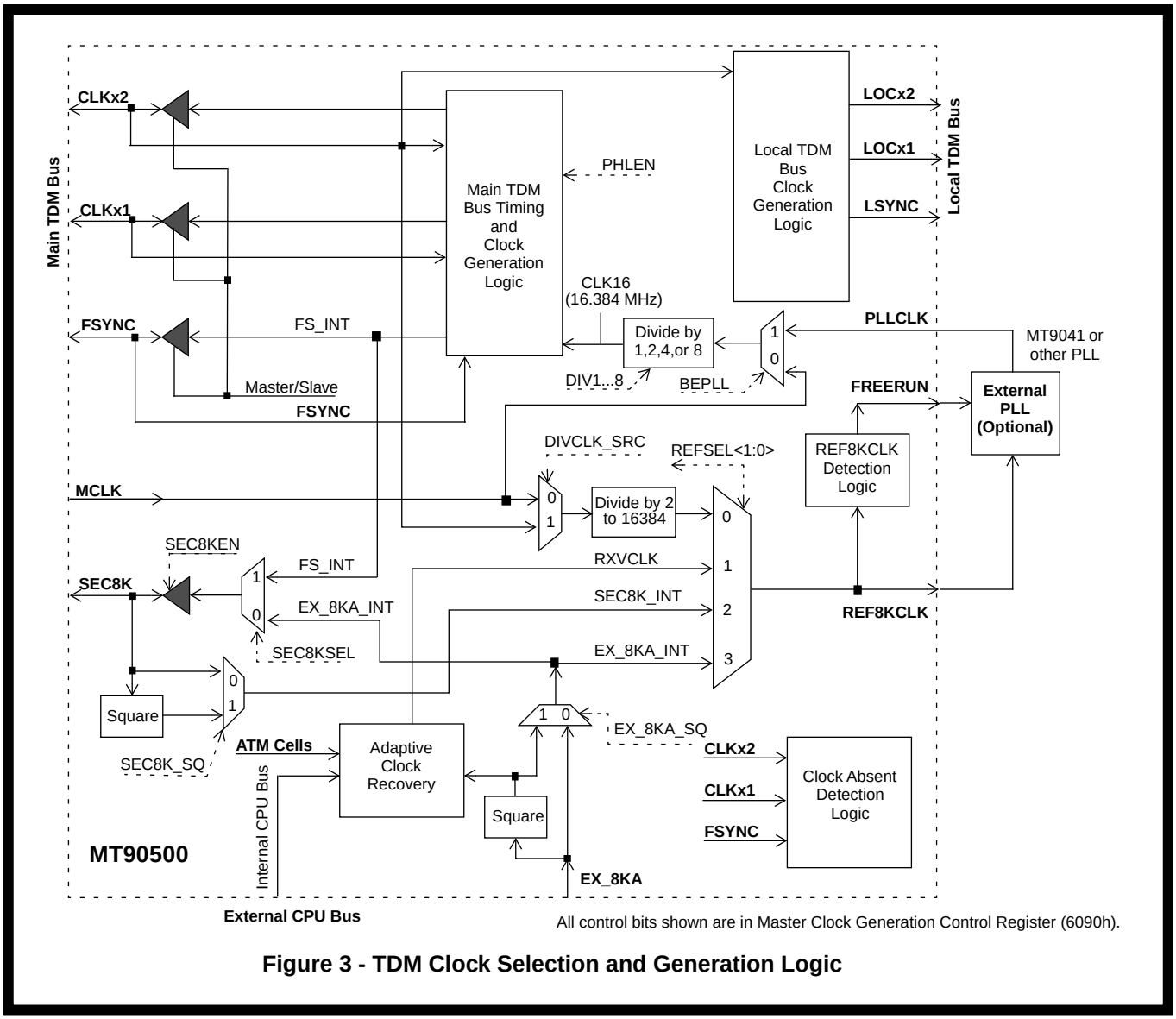


Figure 3 - TDM Clock Selection and Generation Logic

- The CLKx2 signal can be selected as single-ended or differential. (Differential CLKx2 allows compatibility with the H-MVIP bus.) In TDM Timing Slave, the CLKx2 signal can be input on the CLKx2 pin, or the differential CLKx2PI and CLKx2NI pins. This selection is made with CLKTYPE in the TDM Bus Type Register at address 6010h. In TDM Timing Master, the CLKx2 signal is output on the CLKx2/CLKx2PO pin, and an inverted clock is available on the CLKx2NO pin.

The MT90500 supports the following TDM timing modes:

- **TDM Timing Bus Slave - CLKx2 Reference** (CLKMASTER = '0' in TDM Bus Type Register at 6010h)

In this mode, the MT90500 is configured as a TDM Timing Slave and all internal TDM timing is synchronized to the TDM clock inputs: CLKx2, CLKx1, and FSYNC. The following sub-modes are also selectable:

- The CLKx1 can be an input at the CLKx1 pin, or it can be derived internally from CLKx2. This is controlled by TCLKSYN (address 6010h). If the CLKx1 pin is not used as an input in TDM Slave mode, it remains high-impedance.
- TDM Timing Slave operation takes its 8 kHz framing from the FSYNC input pin, which would usually be driven by the TDM bus. To support other implementations, the REF8KCLK output remains active in TDM Slave mode. An 8 kHz reference output can be made available at REF8KCLK, selectable from the EX_8KA input, the SEC8K pin, or one of the internal dividers. In addition, the FREERUN output can be used to monitor the presence of REF8KCLK.

- **TDM Timing Bus Master - Freerun** (CLKMASTER = ‘1’ in TDM Bus Type Register at 6010h)

In this mode, the MT90500 is configured as the TDM Timing Master and the MT90500 drives the three TDM bus clocks: CLKx2, CLKx1, and FSYNC. The MT90500 clock generator block uses either the MCLK input or the PLLCLK input to generate all of the required clocks. Typically in this mode MCLK or PLLCLK is connected to an oscillator, and no other synchronization source is used. Several selections must be made:

  - The selection of MCLK or PLLCLK is determined by the BEPLL bits in the Master Clock Generation Control Register at 6090h.
  - The selected clock is divided by 1, 2, 4, or 8 to obtain a 16.384 MHz clock, called CLK16. This division is controlled by the DIV1...8 bits at 6090h.

- **TDM Timing Bus Master - 8 kHz Reference** (CLKMASTER = ‘1’ in TDM Bus Type Register at 6010h)

In this mode, the MT90500 is configured as the TDM Timing Master and the MT90500 drives the three TDM bus clocks, synchronized to one of several possible 8 kHz references. Typically, in this mode, the PLLCLK input is driven by an external PLL (such as the Mitel MT9041), which is controlled by the REF8KCLK and FREERUN outputs. The following options are also selectable:

  - One of four 8 kHz reference sources must be selected, using the REFSEL bits at 6090h. (See Figure 3 and Section 4.1.1.2 for further details.)
  - If the external PLL is controlled by the FREERUN output pin, the pin’s operation must be specified by the FREERUN bits at 6090h. The CPU can force the FREERUN pin to either state, or allow the FREERUN pin to follow the REF8KCLK failure-detection bit (REFFAIL at 6082h).

- **Bus Master-Alternate** (CLKMASTER = ‘0’, CLKALT = ‘1’ in TDM Bus Type Register at 6010h)

In this mode, the MT90500 is configured as a TDM Timing Slave, but stands ready to become the Timing Master, should the timing on the TDM bus fail. The switch is normally automatic (based on the CLKFAIL input), but can also performed by the CPU (for instance: by programming the chip into TDM Timing Master following a Clock Absent interrupt). The following options are also selectable:

  - To make the switch from Alternate to Master automatic, several settings are required: CLKALT at 6010h is set HIGH, and the CORSIGA pin is configured as the CLKFAIL input (CORSIGACNF = “11” at 6004h).
  - The Master-Alternate operates normally as a TDM Timing Slave, and has the same options as the TDM Timing Slave listed above.
  - The Master-Alternate can be set up to switch to Master-Freerun operation, should the TDM bus clocks fail. The same options as listed above for Master-Freerun apply to this mode.
  - The Master-Alternate can be set up to switch to Master-8 kHz Reference operation, should the TDM bus clocks fail. The same options as listed above for Master-8 kHz Reference apply to this mode. Additionally, REF8KCLK can be obtained from the TDM bus by dividing CLKx2. This allows the external PLL to be phase-locked to the TDM bus clocks. Note that in this case the FREERUN output should be set up to automatically place the external PLL in freerun should the TDM bus clocks fail.
  - The internal 8 kHz (FS_INT) of the Master-Alternate can be phase-locked to the TDM bus FSYNC by setting PHLEN = ‘1’ at 6090h. (This is only valid when the FSYNC type at 6010h is set to “00”.) This will align the internal “stand-by” FSYNC, CLKx2, and CLKx1 to the TDM bus to within a clock cycle of the internal 16.384 MHz clock, allowing for minimal phase-shift should the Master-Alternate MT90500 take over the TDM bus clocks.

4.1.1.2 REF8KCLK Selection Logic

The REF8KCLK output pin of the MT90500 is intended to provide a clock reference to an optional external PLL. This signal would usually be an 8 kHz frame pulse, but other signals are possible. The external PLL (e.g. Mitel MT9041) can be used to multiply the REF8KCLK output to 16.384 MHz (or 32.768 MHz) and attenuate jitter. The 16.384 MHz can then be applied to the PLLCLK input pin to allow the MT90500 to generate the TDM clocks: CLKx2, CLKx1 and FSYNC. The source for the REF8KCLK signal is selected via the REFSEL bits at address 6090h. The four possible sources for REF8KCLK are:

  - a clock input signal pin operating at 8 kHz (EX_8KA)

- a secondary 8 kHz reference from the TDM bus (SEC8K, compatible with MVIP/H-MVIP)
- a freerun mode clock, which is a divided-down version of CLKx2 or MCLK; selected by DIVCLK_SRC in register 6090h, and divided as specified in register 6092h
- RXVCLK, a more precisely divided-down version of MCLK from the Adaptive Clock Recovery block. The division is controlled by registers 60A8h and 60AAh.

The REF8KCLK signal is made available on the output pin whether the MT90500 is programmed to be TDM Timing Master or Slave.

Also included in the MT90500 is circuitry to convert the SEC8K signal and the EX_8KA signal into square waves. If the SEC8K_SQ control bit in register 6090h is set HIGH, internal logic will convert the SEC8K input signal into a square wave before passing it to the REF8KCLK selection mux. The EX_8KA_SQ bit controls the squaring function for the EX_8KA signal. See the register 6090h. Mitel PLLs will typically work with either a pulse 8 kHz, or a square 8 kHz, but other PLL implementations may require a square 8 kHz reference input.

4.1.1.3 Main TDM Bus Timing and Clock Generation Logic

When the MT90500 is in the TDM Timing Master mode, this logic generates the main TDM bus clocks (CLKx2, CLKx1, and FSYNC). This block receives CLK16 (a 16.384 MHz clock which is a divided-down version of either PLLCLK or MCLK, as set in register 6090h) and outputs the generated TDM bus clocks. By programming the appropriate software registers (i.e. TDMTYP at address 6010h), the generated signals can be 16.384MHz/ 8.192MHz/4.096MHz, 8.192MHz/4.096MHz/2.048MHz, and 8 kHz respectively. Additionally, the TDM Bus Clock Generation Logic generates a source signal to the SEC8K output line when the SEC8KEN register bit is enabled.

When in TDM Timing Slave mode, or in Master-Alternate mode, this logic generates an internal stand-by 8 kHz signal (FS_INT), from the clock selected by BEPLL in register 6090h. This can be driven out on SEC8K if enabled by SEC8KEN.

4.1.1.4 TDM Clock Drivers

If the MT90500 is the TDM Timing Master, this block enables the clock drivers for CLKx2, CLKx1, and FSYNC. If the MT90500 is in Slave mode, the drivers are disabled and CLKx2, CLKx1, and FSYNC are inputs to the MT90500. In Slave mode, the CLKx1 source can be separately selected between the CLKx1 input or internally provided CLKx2/2. These options are controlled by the TDM Bus Type Register at 6010h.

4.1.1.5 Clock Failure Detection

There are three status bits related to the detection of clock failure: REFFAIL (6082h), and CABS and CFAIL (6002h). These bits will cause an interrupt if their respective enable bits are set (REFFAILIE at 6080h, and CABSIE and CFAILIE at 6000h) and the TDM_INTE bit is set at 0000h.

The REFFAIL bit monitors the absence of the REF8KCLK signal. When this signal is absent, the clock detect logic can activate the FREERUN output signal which is used to place the external PLL in freerun mode. Once the REF8KCLK signal goes back to normal (due to the CPU changing the timing source), the CPU can disable the FREERUN output signal by clearing the REFFAIL bit in the Clock Module General Status Register at 6082h. With proper selection of the external PLL, this clock failure detection circuit can help to guarantee that the TDM clocks do not glitch when the REF8KCLK reference to the external PLL changes.

The CABS bit indicates that one or more of the TDM bus clock signals (CLKx2, CLKx1, or FSYNC) are absent. This block uses MCLK to check for activity on the above signals. In the case of clock absence, the Clock Absent (CABS) bit in the TDM Interface Status (TIS) Register at address 6002h is activated.

The CFAIL bit monitors the CLKFAIL pin (a SCSA bus signal) and requires that the CORSIGA pin be configured as the CLKFAIL input. If the CLKFAIL input goes HIGH when the MT90500 is operating in Master-Alternate mode (CLK_ALT at 6010h), the MT90500 will take over the TDM bus and become the Master TDM clock source (see the Bus Master-Alternate description in Section 4.1.1).

4.1.2 TDM Interface Operation

4.1.2.1 Main TDM Bus Operation

The main TDM bus (pins ST[15:0]) supports SCSA, MVIP, H-MVIP, ST-BUS, and IDL protocols. These buses have different frame sync pulse orientations and different data sampling specifications, as well as different pin requirements. However, all of these buses are composed of 16 data pins, as well as CLKx2, CLKx1, and FSYNC lines.

The TDM bus type is controlled by the TDM Bus Type Register at 6010h. In all bus types, outputs change on the rising edge of CLKx1. Inputs can be sampled at the 2/4, 3/4 or 4/4 point of the CLKx1 signal. MVIP/SCSA/ ST-BUS all use a negative FSYNC that is asserted for one CLKx2 cycle, straddling the frame boundary. The IDL bus uses a positive FSYNC which is asserted for one cycle of CLKx1, preceding the frame boundary. (See Figure 35, “Nominal TDM Bus Timing,” on page 102.)

4.1.2.2 TDM Loopback

The General Output Enable bit (GENOE in the TDM Interface Control Register at 6000h) is used to enable data to be driven out on the TDM output streams. When this bit it not set (i.e. it is LOW), the internal TDM transmit buses are connected to the internal TDM receive buses (while the internal TDM buses are disconnected from the external TDM buses) giving a TDM loopback from ATM receive back to ATM transmit. In this mode, the internally-generated TDM clocks and synchronization signals are used. This allows the user to test the MT90500 in stand-alone mode by passing receive ATM cells through the SAR, through the internal loopback at the TDM interface, and back through the SAR and out as transmit ATM cells.

4.1.2.3 Per-channel Output Enable Feature

The ST[15:0] pins are bidirectional, and are able to switch between input and output directions on a per-channel basis. The Output Enable Registers located at addresses 7000 + 2N (N = 0, 1, ..., 127) are used for individual time slot output enable control. Depending on the TDM bus rate, up to 128 registers (256 bytes) are used to provide up to 2048 individual channel-output-enable bits. At 2.048 Mbps, 32 registers are used; at 4.096 Mbps, 64 registers are used; and at 8.192 Mbps, 128 registers are used.

During each channel period (TDM time slot), 16 output enable bits (one register) are read from the Output Enable Registers. Within each frame, 32, 64, or 128 registers are read (depending on the TDM bus rate). The GENOE bit must be set HIGH, as well as the individual channel-output-enable bit, in order for a TDM channel to be transmitted from the MT90500 onto the TDM bus. In order to prevent data collisions on the TDM bus, the user should clear all Output Enable Register bits for channels not used as outputs, prior to setting the GENOE bit. The GENOE signal, when inactive, asynchronously deactivates the tristate buffers on the data pins and routes the output paths back into the input paths, causing the TDM bus to enter the TDM Loopback mode (see Section 4.1.2.2).

Since the ST pins are bidirectional, the input sampling is always active and output data can be re-sampled back into the MT90500. This re-sampling is used when LOCSTi channels are output on a ST pin and then re-sampled for ATM transmission, when ST outputs are re-sampled for transfer to the LOCSTo pin, or for test and verification purposes.

4.1.2.4 Local Bus Operation

The local bus signals are:

- LOCx2, LOCx1, LSYNC - clock output signals;
- LOCSTi, LOCSTo - Local Serial TDM data in and data out.

The MT90500 provides three output clocks for the local TDM bus: LOCx2, LOCx1 and LSYNC. These clocks are derived from CLKx2, and controlled by the relevant bits in the Local Bus Type Register (register 6020h). The LCLKDIV bits allow LOCx2 to be equal to CLKx2, CLKx2 / 2, or CLKx2 / 4 (note that the local bus rate is 2.048 Mbps, which is always equal to, or less than, the main TDM bus rate). Also in register 6020h are the control bits to select the LSYNC frame-pulse type, the routing of TDM streams onto and from the local bus, and the LOCSTi sampling point.Except for the rate, the local bus type can be configured independently of the main TDM bus type.

4.1.2.5 Local Bus Data Transfer Process

A local bus data transfer process is provided, which allows local serial TDM input (LOCSTi) data to be output on the main TDM bus (ST[15:0]) in place of the usual data from the internal frame memory. Similarly, data from the main TDM bus can be routed directly onto the local TDM output (LOCSTo), without affecting the TDM to internal frame memory transfer.

The local bus pins on the MT90500 are an extension of the main TDM bus. The data on any stream of the main TDM bus may be passed to the local bus output (LOCSTo). The source pin (one of ST[15:0]) is controlled with the STi2LOCSTo bits at 6020h, and the time slots to be transferred are indicated by the TDM Bus to Local Bus Transfer Register (6022h). Note that this TDM data can be from two sources: either externally-sourced data being driven into the selected ST pin, or data from the ATM link being driven out by the RX_SAR, and copied to the LOCSTo pin. When fewer than the maximum number of available time slots are transferred between the main TDM bus and the local bus, the unused LOCSTo output time slots are filled with data fed back internally from LOCSTi.

Similarly, the data input on LOCSTi may be passed to any stream of the TDM bus as indicated by the Local Bus to TDM Bus Transfer Register (6024h), and the LOCSTi2STo bits at 6020h. Note that when the local bus to TDM process is enabled, from 1 to 32 data bytes from the RX_SAR will be replaced by local bus data. The enable bits for the main TDM bus channels are the normal bits in the Output Enable Registers (7000h + 2N). Data from the LOCSTi input pin can be transferred to the ATM link through the TX_SAR, by re-sampling the channels on which the local bus data is output as inputs to the TX_SAR.

4.1.3 TDM Data to External Memory Process

4.1.3.1 General

The segmentation of serial TDM input data into ATM cells starts by copying the TDM data into Transmit Circular Buffers. The data is then read out of the Transmit Circular Buffers by the TX_SAR (see Section 4.3.2, “TX_SAR Process,” on page 43). The initial step of copying the serial TDM input data into the Transmit Circular Buffers is performed by the TDM Data to External Memory Process described in this section.

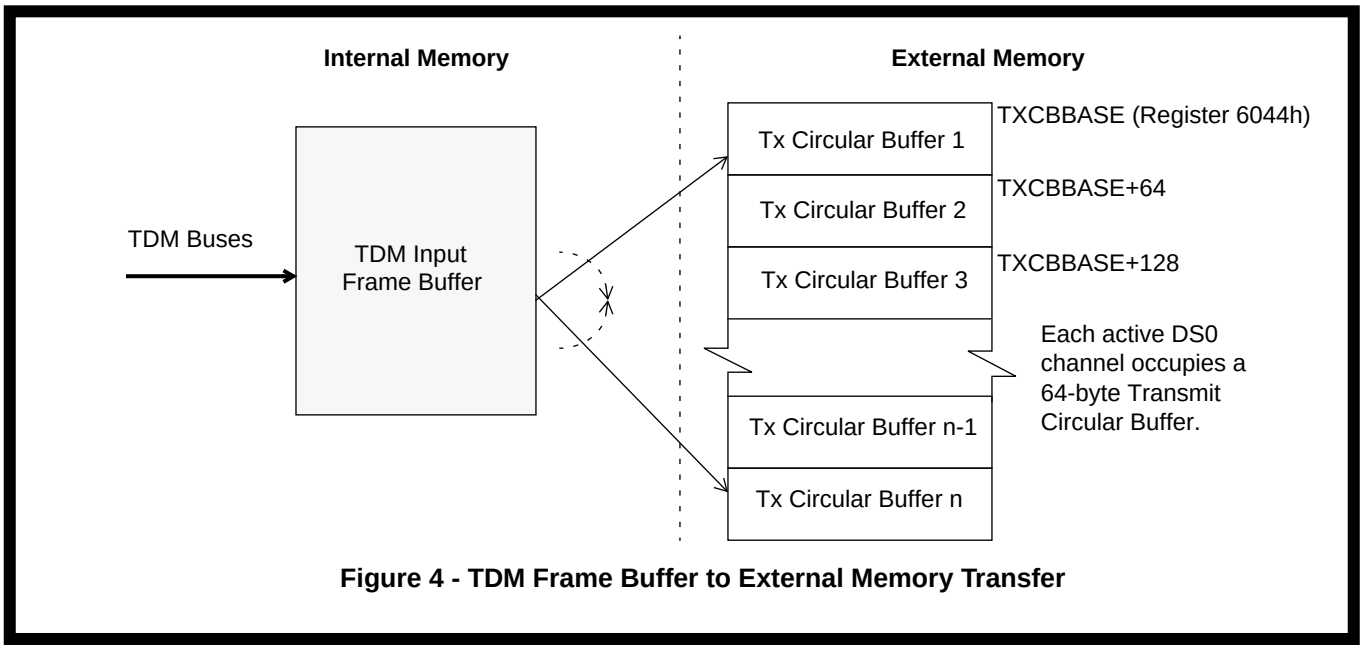


Figure 4 - TDM Frame Buffer to External Memory Transfer

All of the serial TDM input data available on the TDM buses is first written to an internal frame buffer which holds 4 frames of TDM data per input channel. As shown in Figure 4, this internal frame memory (which is used in both the receive and transmit directions simultaneously) is used as a pingpong buffer. While one page of the memory is being loaded with input TDM data, the other page of the memory is being transferred to the Transmit Circular Buffers in external memory. This transfer occurs every 500 µs (4 frames * 125 µs per frame).

4.1.3.2 Transmit Circular Buffer Control Structures

To minimize the amount of external memory required for the TDM Data to External Memory Process, only the TDM channels assigned to be transmitted over the ATM link are transferred to external memory. Each TDM channel to be transmitted over the ATM link occupies a 64-byte Transmit Circular Buffer in external memory. As shown in Figure 5, the MT90500 fetches control data from the Transmit Circular Buffer Control Structure in external memory in order to determine which TDM channels to transfer to external memory and where to put the data. The Transmit Circular Buffer Control Structure is a sequential control table consisting of 16-bit entries:

- Bit<15> indicates that the entry is valid (active HIGH).
- Bits<14:11> are not used, and should be set to zeroes.
- Bits<10:0> identify a channel number.
    - Bits<10:4> identify a TDM channel within a stream. The channels are numbered from 0 to 127.
    - Bits<3:0> identify a stream number, from 0 to 15.

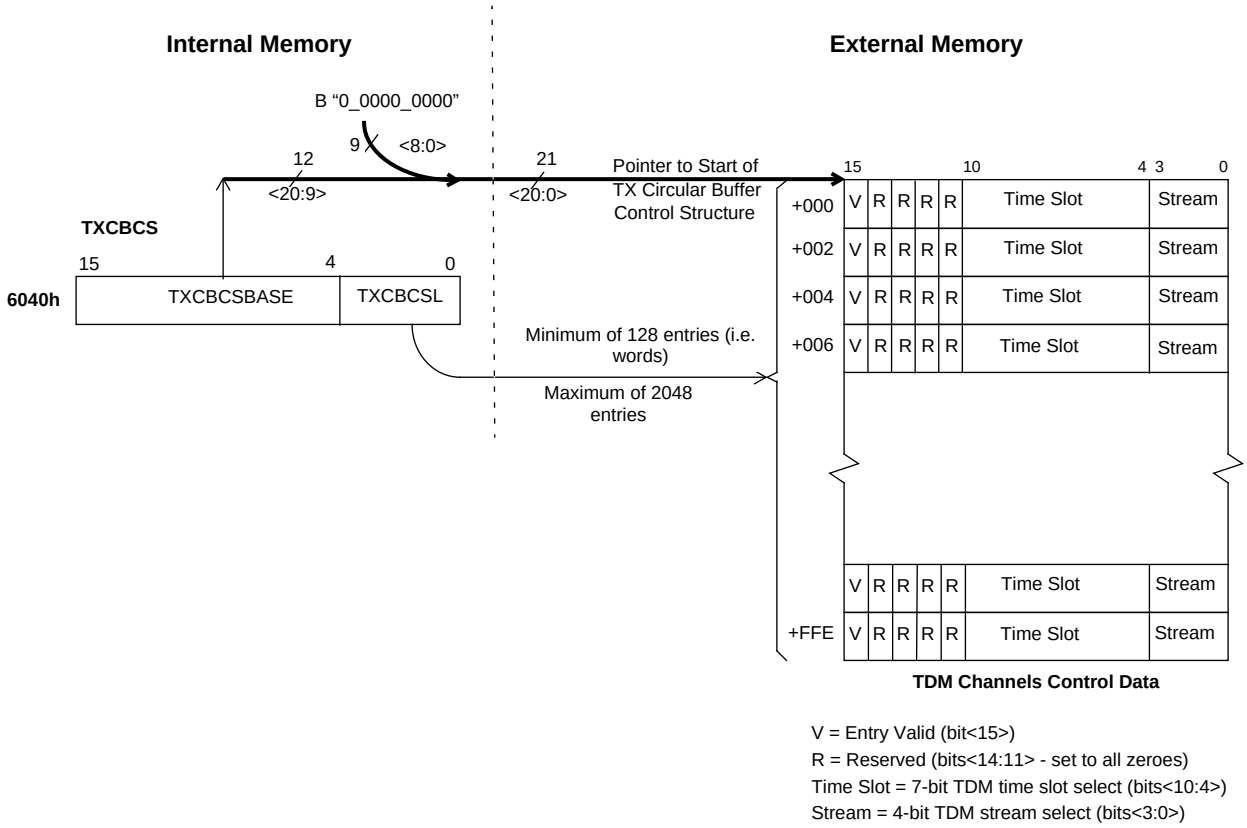


Figure 5 - Transmit Circular Buffer Control Structure

The first entry in the Transmit Circular Buffer Control Structure tells the hardware from which TDM channel it will fill the first 64-byte Transmit Circular Buffer, the second entry tells the hardware from which TDM channel it will fill the second Transmit Circular Buffer, and so on. If the entry is not valid (i.e. the V bit is not asserted), the transfer is not executed. In order to prevent unnecessary transfer of TDM data to external memory, the user should zero-out all unused entries within the TX Circular Buffer Control Structure.

4.1.3.3 Transmit Circular Buffers

The location of the Transmit Circular Buffers in external memory is determined by TXCBBASE (TX Circular Buffer Base Address), found in register 6044h. The first Transmit Circular Buffer is located at TXCBBASE. The second is located at TXCBBASE + 64, the third at TXCBBASE + 128, etc., as seen in Figure 4. All Transmit

Circular Buffers are 64 bytes long, so buffer addresses are not included in the control structure but are considered to follow each other linearly, one after the other, corresponding to the order of the entries in the control structure. Therefore, if the base address of the TX Circular Buffers was 10000h (as defined by the TXCBBASE entry at 6044h), the first entry in the control structure (be it valid or not) would correspond to the buffer at 10000h, the next to 10040h, the one after to 10080h, etc.

The last step of the TDM Data to External Memory Process transfers data from the internal frame buffer to the Transmit Circular Buffers in external memory. The write pointer to all Transmit Circular Buffers is a single 8-bit counter that increments every four frames as the Internal to External Memory transfer is performed. The 4 least significant bits in this counter are used as the TDM Circular Buffer Write Pointer. All the desired TDM channels in the internal frame buffer will be transferred into the Transmit Circular Buffers as specified by the Transmit Circular Buffer Control Structure. Note that the Transmit Circular Buffer Control Structure must be initialized before the Internal/External Memory Process is enabled (via the IEENA bit in register 6000h).

4.1.4 External Memory to TDM Data Output Process

4.1.4.1 General

The reassembly of received CBR (Constant Bit Rate) ATM cells into serial TDM output data is completed by reading the data out of Receive Circular Buffers and placing the data on the TDM outputs. The data is written to the Receive Circular Buffers by the RX_SAR (see Section 4.4.2, “RX_SAR Process,” on page 53). Then the reading of serial TDM output data from the Receive Circular Buffers is performed by the External Memory to TDM Data Output Process. This process will be outlined here.

The same internal frame buffer used in the TDM Data to External Memory Process is used to buffer the received data to be transferred to the TDM output bus. As shown in Figure 6, this internal frame buffer holds 4 frames of output data for each TDM channel (to a maximum of 2,048 channels). This frame buffer is used in a pingpong scheme where alternately half the memory is used to transfer data to the TDM buses while the other half is being used to transfer data from the external memory. TDM data is transferred from the Receive Circular Buffers in external memory to the internal frame buffer. As in the TDM Data to External Memory Process described previously, the pointer to all Receive Circular Buffers is a single 8-bit counter that increments every four frames as the External to Internal Memory transfer is performed. The least significant 4 to 8 bits of the counter are used as the TDM Circular Buffer Read Pointer, depending on the size of the Receive Circular Buffers.

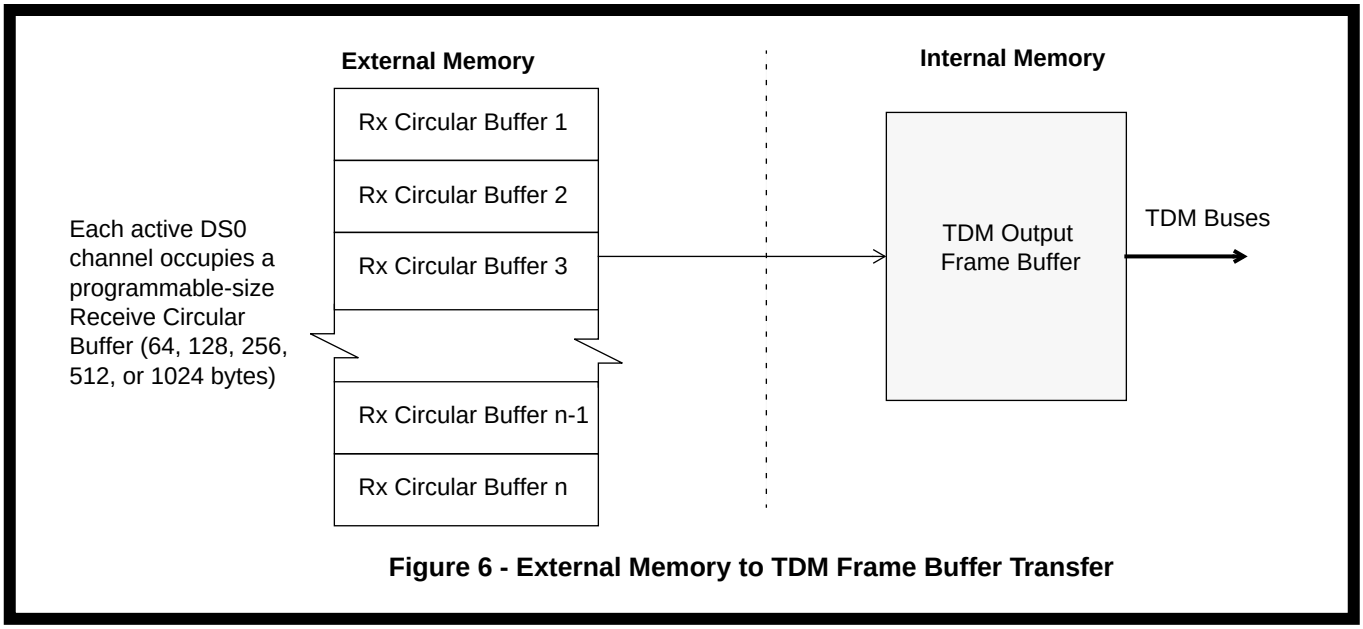


Figure 6 - External Memory to TDM Frame Buffer Transfer

4.1.4.2 External Memory to Internal Memory Control Structures

To know which internal frame buffer TDM channels need to be written (generally, only the TDM channels scheduled for transmission on the TDM bus), the MT90500 uses control data from the External to Internal Memory Control Structure. The External to Internal Memory Control Structure is located in external memory,

and is depicted in Figure 7. The control data in the External to Internal Memory Control Structure tells the hardware where in external memory the receive data is located (Rx Circ. Buf. Address), the size of the Receive Circular Buffer used, and to which TDM channel (TDM Channel #) this data must be written.

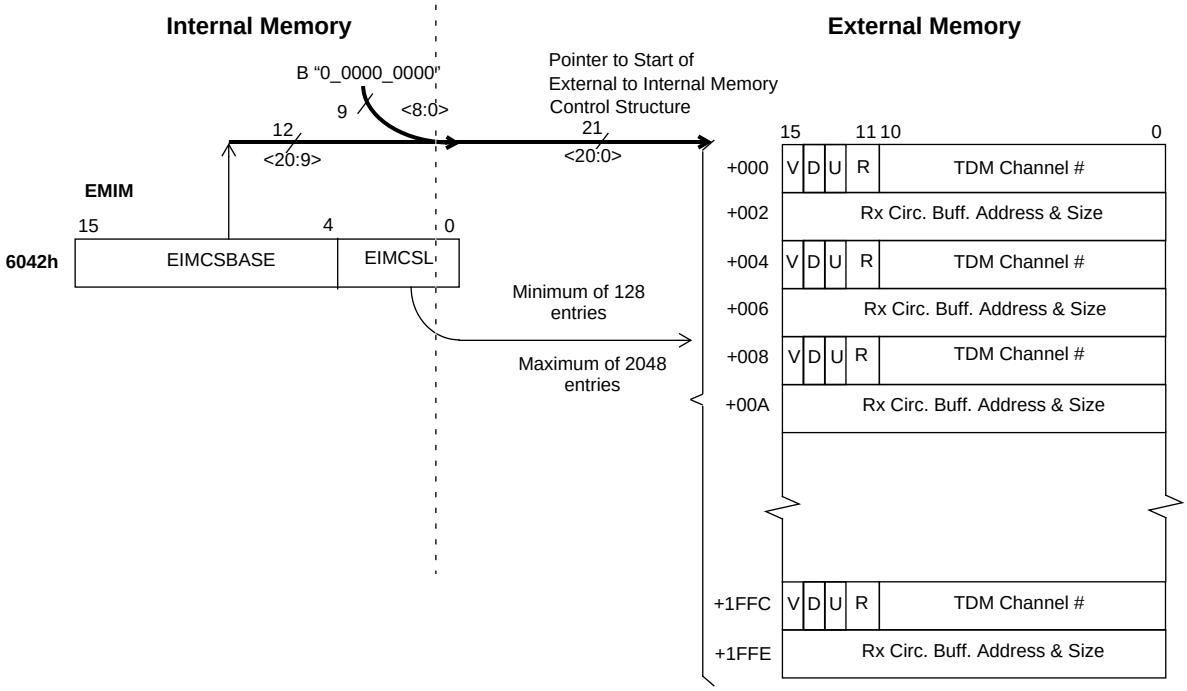
The External to Internal Memory Control Structure uses a 32-bit control word, as indicated below and in Figure 7:

- Bit<15> - V - indicates that the entry is valid (active HIGH). If the entry is not valid, it is simply bypassed and the next entry is read.
- Bit<14> - D - Write-back disable bit. If HIGH, the receive TDM data will be left unaltered in the Receive Circular Buffer. If LOW, FFh will be written over each byte of the receive TDM data once it has been transferred to the internal frame memory. (This has the effect of putting FFh - silence - on the TDM bus if the Receive Circular Buffer underruns and the same byte is read again before new TDM output data is written to the Receive Circular Buffer by the RX_SAR.)
- Bit<13> - U - TDM Read Underrun detection enable. If this bit is HIGH, and the External Memory to Internal Memory Process tries to transfer a byte which has already been transferred, an underrun event is detected and an interrupt may be generated. See registers 6000h, 6002h, 6046h and 6048h.
- Bits<12:11> - R - Not used.
- Bits<10:0> - TDM Channel # - identifies a destination TDM channel number and stream
    - Bits<10:4> identify a TDM channel within a TDM stream. The channels are numbered from 0 to 127.
    - Bits<3:0> identify a TDM stream number, from 0 to 15 (corresponding to the ST[0:15] pins).
- Rx Circ. Buff. Address and Size - indicates the Receive Circular Buffer address, and the size of the Receive Circular Buffer (64, 128, 256, 512, or 1,024 bytes). The leading bits in the field, when appended by a number of least-significant zeroes, indicate the Receive Circular Buffer address. The total number of bits representing an address should be 21 bits. For example, for a 128-byte buffer, the 14-bit address given in the structure will be appended by 7 zeroes, resulting in a 21-bit address.

It is important to consider this control structure when determining the location of Receive Circular Buffers in external memory. Examining the configuration shown in Figure 7 on the next page, it can be seen that the number of bits available to identify the address of Receive Circular Buffers differs depending on the size of the buffer. Due to this restriction, it is essential that each buffer be located only on a boundary corresponding to the size of the buffer (i.e. 64-byte buffers must be located on 64-byte boundaries, 128-byte buffers must be located on 128-byte boundaries, and so on...).

Once all of the entries have been scanned, the internal frame memory is filled and the External Memory to Internal Memory process terminates. If the process is still active four frames after being started, a “TDM Out of Bandwidth Error” (found in the TDM Interface Status Register at 6002h) is generated.

The final step is for the MT90500 to drive the TDM data out on the TDM pins, ST[15:0]. Since not all time slots are designated as outputs, separate Output Enable Registers located at addresses 7000 + 2N (N = 0, 1, ..., 127) are used for individual time slot output enable control. In addition, the GENOE bit in the TDM Interface Control Register at 6000h must be set HIGH to enable the general Internal Memory to TDM Output Process (see Section 4.1.2.3 for more details).



Structure of the Receive Circular Buffer Address and Size Fields

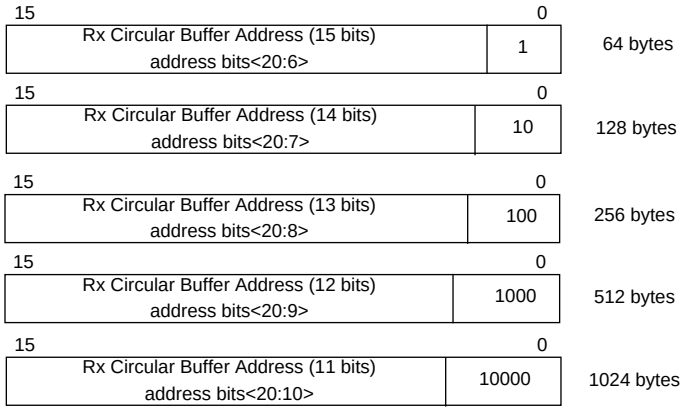


Figure 7 - External Memory to Internal Memory Control Structure

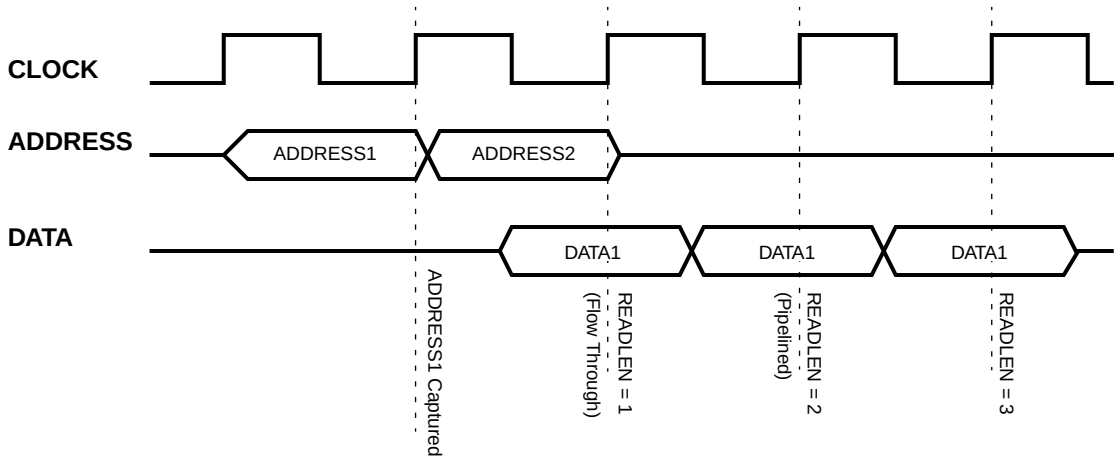
4.2 External Memory Controller

The external memory controller block of the MT90500 resides between the internal blocks and the external memory. It receives memory access requests from the internal blocks (TDM Interface, TX_SAR, RX_SAR, UTOPIA, and Microprocessor modules) and services them by reading data from, or writing data to, the external memory. The MT90500 pins connecting to the external memory consist of: 18 address bits (MEM_ADD[17:0]), 4 memory bank/chip selection bits ($\overline{\text{MEM\_CS}}$[1:0][H/L]), 32 data bits (MEM_DAT[31:0]), 4 parity bits (MEM_PAR[3:0]) used as TDM Read Underrun flags, 4 write enable bits ($\overline{\text{MEM\_WR}}$[3:0]), a memory output enable bit ($\overline{\text{MEM\_OE}}$), and a memory clock (MEMCLK). The external memory controller block ensures the proper timing of all memory signals and the flow control of the external memory's data bus. The external memory controller block also converts a 21-bit internal byte-oriented address to a memory bank selection and a physical address. (The 2 LSBs select one byte within the 4-byte/double-word wide data bus, up to 18 bits select a particular double-word address, and the MSB selects one of two possible memory banks.)

The external memory controller block implements memory accesses to an external 36-bit Synchronous Static Random Access Memory (SSRAM or Sync SRAM). It supports one or two banks of external memory, each bank having a total capacity ranging from 32K x 36 bits to 256K x 36 bits. Thus the MT90500 can operate with external memory ranging from 128 Kbytes to 2,048 Kbytes.

The external memory controller can interface with several different types of Sync SRAM, but they must support synchronous bus enabling. Synchronous bus enabling means that the Sync SRAM chip must ONLY enable its data output buffers one cycle after a read (two cycles for pipelined SSRAM), regardless of the state of the asynchronous output enable pin ($\overline{\text{MEM\_OE}}$). A read is indicated by $\overline{\text{MEM\_WR}}$[3:0] all HIGH, and the appropriate $\overline{\text{MEM\_CS}}$[1:0][H/L] asserted. The SSRAM must also support single cycle writes ("early" write, or $\overline{\text{ADSC}}$ type writes). The SSRAM can be a registered-input type ("Synchronous," "Synchronous Flow-Through," or "Synchronous Burst") or a registered-input/registered-output type ("Synchronous Pipelined"). Although the MT90500 uses the synchronous access feature of these memories, it does not use the burst access features of these memories, since most MT90500 memory accesses are random rather than sequential.

Although write accesses to Synchronous SRAM and to Synchronous Pipelined SRAM are identical, there is a difference in the number of clock cycles before data is returned on the data bus during read accesses. The MT90500 supports memories with 1, 2 and 3 stages of pipelining (see Figure 8). Both 18-bit and 36-bit data bus memories are supported, but in the first case, two chips must be used in parallel to form a 36-bit data bus. Also, two 36-bit wide memory banks can be joined to double the memory's capacity (see Figure 9). Table 9 lists most of the possible memory size combinations. (Note: 16-bit and 32-bit memories can be used, but in that case the TDM Read Underrun indication will not be available.) All chips used must be of the same type.



Note: The number of clock cycles between an address (ADDRESS1) and its read data (DATA1) is set according to READLEN in the Memory Configuration Register at address 0040h. Values greater than 3 are reserved.

Figure 8 - Memory Read Pipeline Length

Byte Address	32K Addressing Mode MEM_ADD[14:0]		64K Addressing Mode MEM_ADD[15:0]		128K Addressing Mode MEM_ADD[16:0]		256K Addressing Mode MEM_ADD[17:0]	
0 - 128K	Bank 1	32K*4bytes	Bank 1	64K*4bytes	Bank 1	128K*4bytes	Bank 1	256K*4bytes
128K - 256K	Bank 2	32K*4bytes						
256K - 384K			Bank 2	64K*4bytes				
384K - 512K								
512K - 640K					Bank 2	128K*4bytes		
640K - 768K								
768K - 896K								
896K - 1024K								
1024K - 1152K							Bank 2	256K*4bytes
1152K - 1280K								
1280K - 1408K								
1408K - 1536K								
1536K - 1664K								
1664K - 1792K								
1792K - 1920K								
1920K - 2048K								

Figure 9 - Logical Byte Address vs. Physical Address and Memory Banks

Note: The addressing mode, which indicates the number of address lines connected to the external memory, is selected via the ADDMODE<1:0> bits in the Memory Configuration Register (0040h). CPBANK in the same register indicates the number of memory chips per bank.

Table 9 - Memory Size Combinations

Total Memory Size	Address Lines Used	Memory Addressing Mode	Memory Chip Size Bank 1	Memory Chip Size Bank 2
64 Kbyte	13:0	32K	64 Kbyte	—
128 Kbyte	14:0	32K	128 Kbyte	—
192 Kbyte	14:0	32K	128 Kbyte	64 Kbyte
256 Kbyte	14:0 15:0	32K 64K	128 Kbyte 256 Kbyte	128 Kbyte —
384 Kbyte	15:0	64K	256 Kbyte	128 Kbyte
512 Kbyte	15:0 16:0	64K 128K	256 Kbyte 512 Kbyte	256 Kbyte —
768 Kbyte	16:0	128K	512 Kbyte	256 Kbyte
1024 Kbyte	16:0 17:0	128K 256K	512 Kbyte 1024 Kbyte	512 Kbyte —
1536 Kbyte	17:0	256K	1024 Kbyte	512 Kbyte
2048 Kbyte	17:0	256K	1024 Kbyte	1024 Kbyte

Because of the bidirectional data bus, some synchronous SRAM devices may require a turnaround cycle. The MT90500 can be programmed to insert a turnaround cycle between a read access and a write access, as required (see Figure 10). Similarly, the MT90500 can be programmed to insert a turnaround cycle between a read access and a read access to the other memory bank. Some memories have an output disable time that is shorter than the output enable time (so a turnaround cycle between reads to different banks is not necessary), meanwhile other memories require a turnaround cycle. This type of turnaround cycle is illustrated in Figure 11.

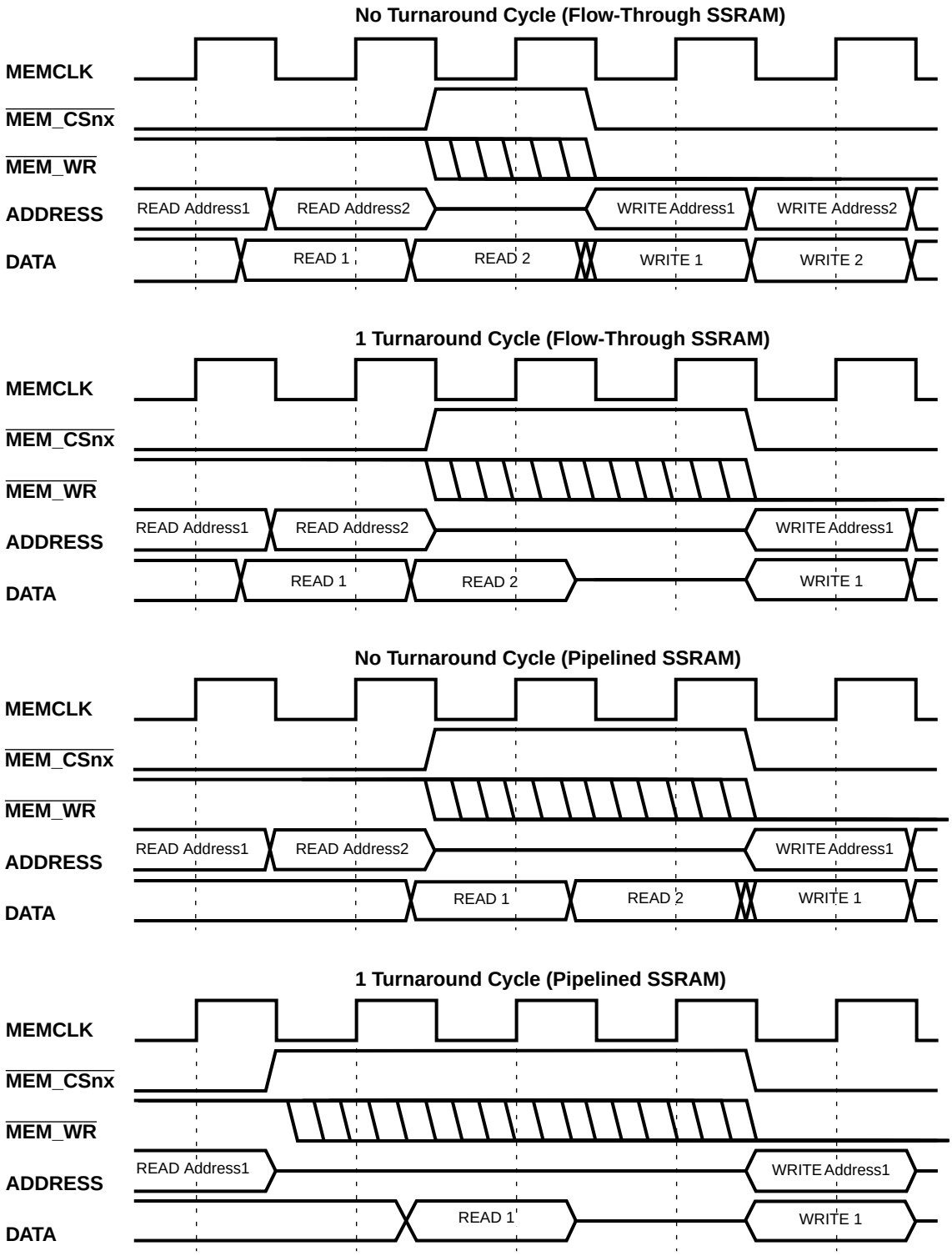


Figure 10 - Read / Write Turnaround Cycles

It should be noted that turnaround cycles, in effect, restrict the memory bandwidth, and therefore the operation of the MT90500. Maximum throughput is achieved with full clock speed on the MCLK input (which drives MEMCLK), and with non-pipelined synchronous SRAM without turnaround cycles (easiest achieved by using a single bank). Maximum throughput is only required in applications requiring a full 1024 transmit TDM and 1024 receive TDM channels and extra CPU accesses for data or frequent setup.

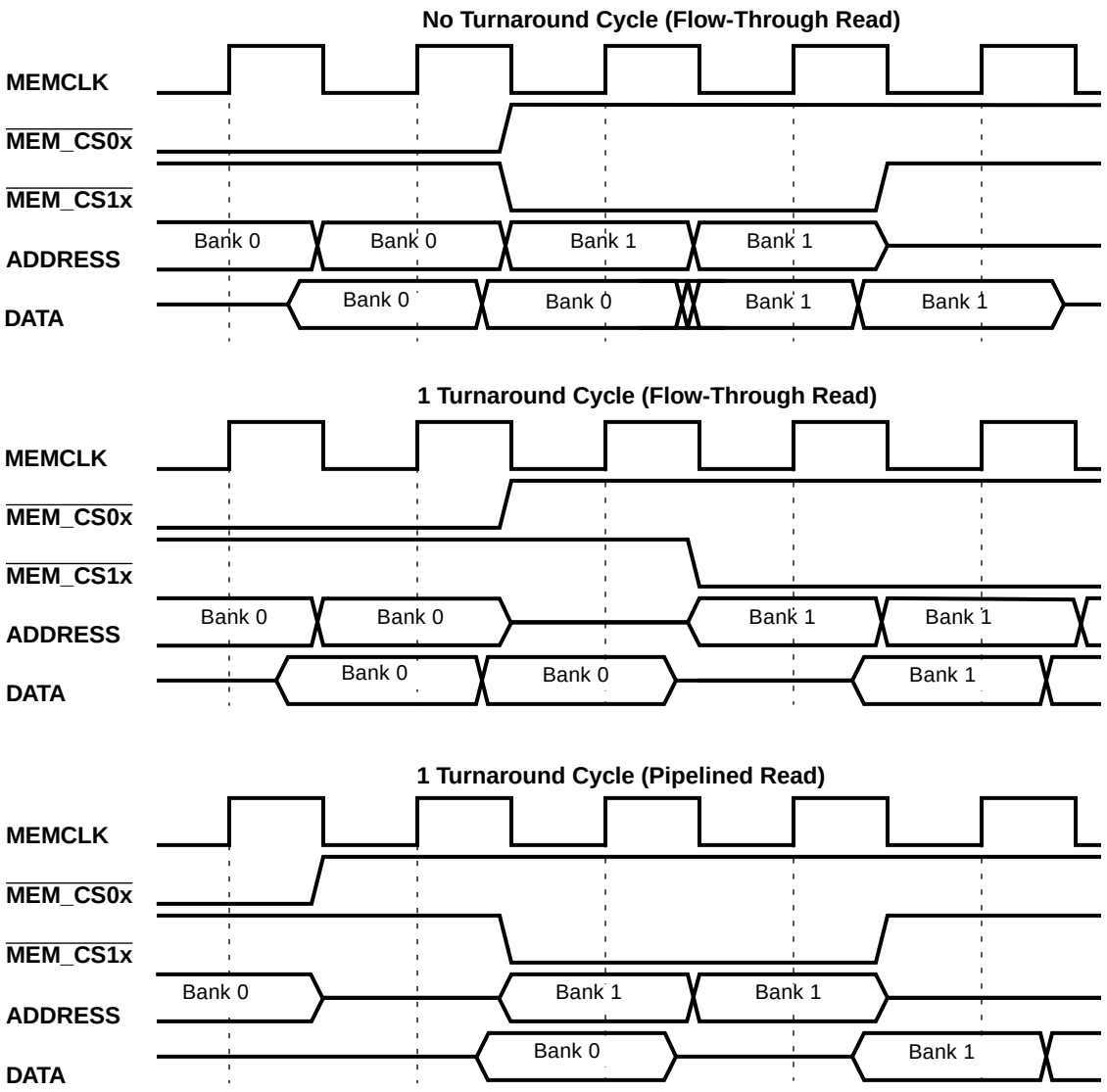


Figure 11 - Read / Read Turnaround Cycles

All of the above features are programmable by the software controlling the MT90500. The Memory Configuration Register (0040h) must be set before any memory process can be enabled. Before any accesses are done to the external memory, the RRTA, RWTA, READLEN, CPBANK and ADDMODE fields in this register must be written and must represent the actual memory configuration.

4.3 TX_SAR Module

4.3.1 TX_SAR Overview

The TX_SAR block is responsible for performing CBR (Constant Bit Rate) cell assembly functions from the TDM port towards the ATM Primary UTOPIA interface, which is typically connected to a PHY device. According to a user-programmable timing algorithm, the TX_SAR circuit fetches data from the Transmit Circular Buffers located in external memory and builds CBR ATM cells (AAL1, CBR-AAL0, or CBR-AAL5) which are subsequently transferred to the MT90500 internal UTOPIA module and then to the Primary UTOPIA port. The TX_SAR block has no direct interface to the pins of the MT90500, but ties together the TDM module and the UTOPIA module. To construct CBR ATM cells, which must be periodically formed at the correct rate, an “event scheduler” is used. To support different cell payload lengths and CBR AAL types, three programmable event schedulers are provided by the TX_SAR to manage the cell transmission timing.

The TX_SAR provides enough bandwidth to allow the transmission of 1024 channels. The RX_SAR allows reception of 1024 channels simultaneously. (For a total device capacity of 1024 bidirectional channels - all 2048 TDM time slots.)

The amount of external memory required to support the TX_SAR process depends on the number of TDM time slots that need to be transmitted, as well as the number of simultaneous VCs. For example, the transmission of 1024 time slots over 1024 simultaneous VCs requires up to 100 Kbytes of external memory for the TX_SAR process. Less memory is required if fewer VC connections or fewer TDM time slots are used.

The AAL1 cell generation process supports TDM transport and trunking over standardized SDT (Structured Data Transfer) with pointer bytes for up to n = 122 TDM channels; over pointerless Structured Data Transfer for n =1; and over partially-filled cells (where n is less than, or equal to, the payload size). The cell parameters are configured through the microprocessor port. Figure 12 below gives examples of the ATM AAL1 cell formats.

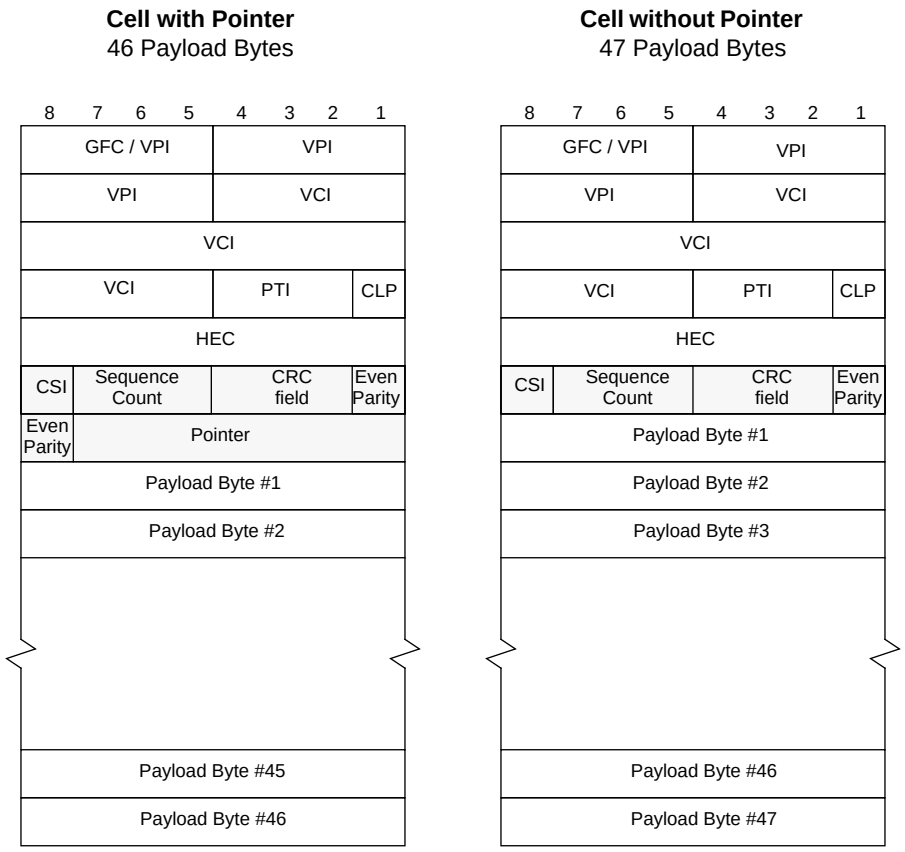


Figure 12 - AAL1 ATM Cell Format

The MT90500 meets the ITU I.363.1 standard for SDT for 1 to 96 octets per structure (1 to 96 TDM channels per VC). The MT90500 meets the ANSI.630 standard for SDT for 1 to 122 octets per structure (1 to 122 TDM channels per VC).

TDM traffic over AAL0 is also supported (referred to in this document as CBR-AAL0). AAL0 is the “bare” or “null” adaptation layer (5 bytes of header plus 48 bytes of direct user payload). Figure 13 shows CBR-AAL0 and AAL1 partially-filled cell formats. In addition, TDM traffic over AAL5 can also be transmitted (referred to in this document as CBR-AAL5). The cell format for CBR-AAL5 is shown in Figure 14.

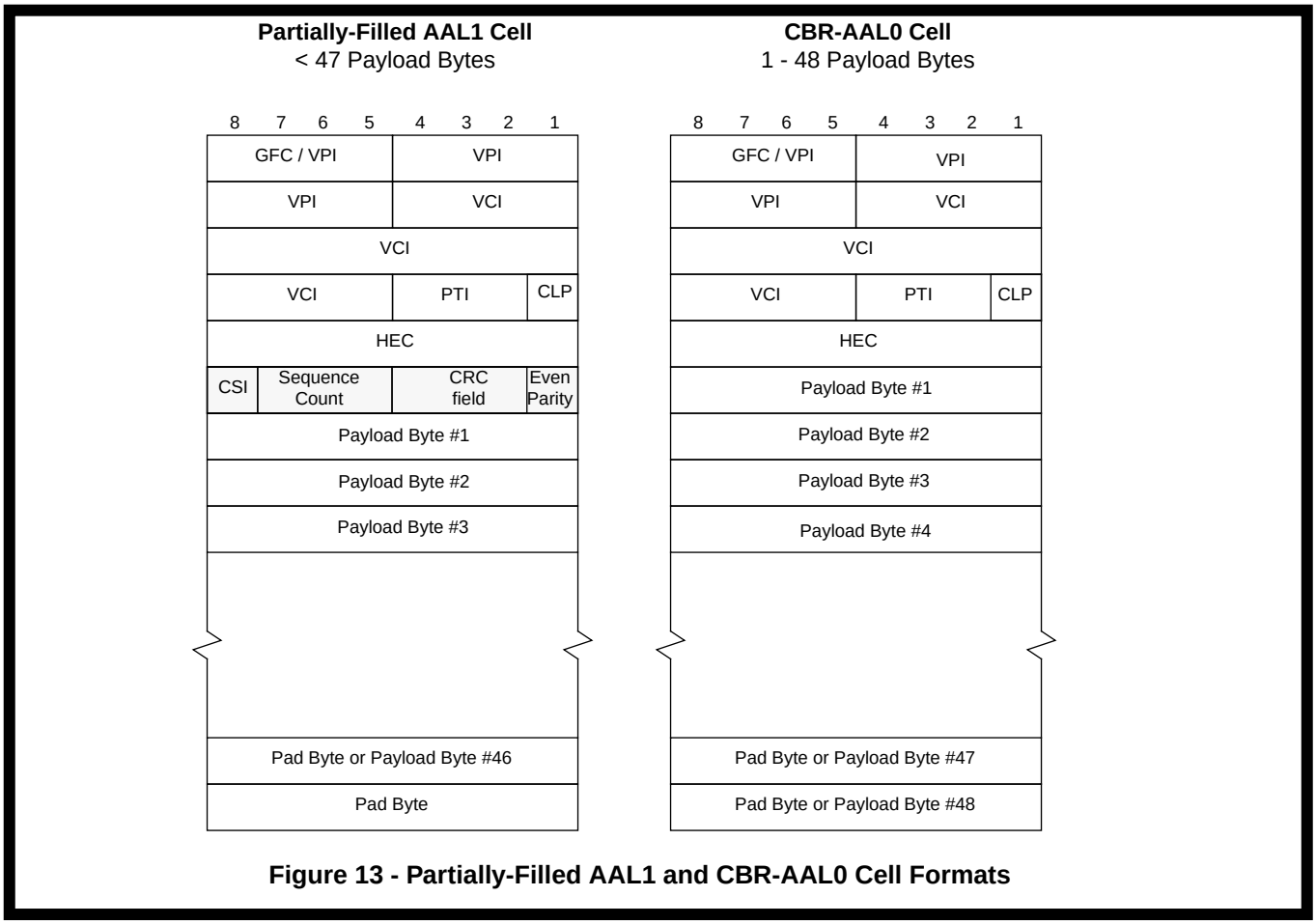
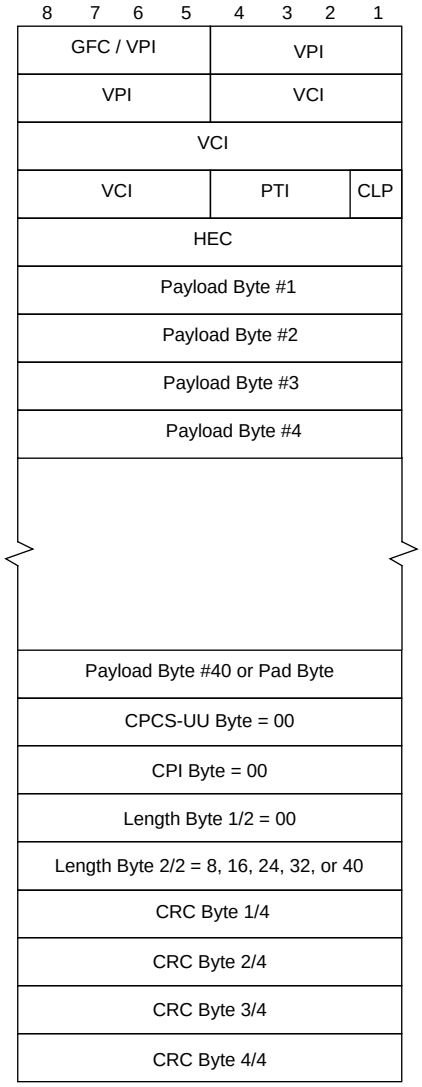


Figure 13 - Partially-Filled AAL1 and CBR-AAL0 Cell Formats

The AAL1 cell differs from the CBR-AAL0 cell in that it contains an AAL1 byte, and it may also contain a pointer byte. The AAL1 byte contains a sequence count (0 to 7), a CSI bit and the SNP (Sequence Number Protection) field. The sequence count is used to identify cell ordering, and to aid in the detection of lost cells. The CSI bit indicates the presence (CSI = 1) or absence (CSI = 0) of a pointer byte in even-numbered cells. In odd-numbered cells, the CSI bits serve to carry the SRTS nibble. The pointer byte indicates the start of the next structure (since structures may be shorter or longer than 47 bytes, and therefore move through the AAL1 payload). Also worth noting is the high-order bit of the header’s PTI field, which can be set to indicate an OAM cell (a cell whose payload contains signalling rather than TDM data).

CBR-AAL5 Cell



- The least-significant bit of the PTI field must be set HIGH to indicate the presence of the CRC-32 bytes (this bit indicates that this is the last cell of a data frame)

- The MT90500 supports 8, 16, 24, 32 or 40 payload bytes. Thus the MT90500 will support N =1 (payload = 8, 16, 24, 32 or 40 bytes) and N = 8, 16, 24, 32 or 40 (payload = N bytes)

Figure 14 - CBR-AAL5 Cell Format

The CBR-AAL5 cell differs from AAL1 and CBR-AAL0 in that its TDM payload is 40 bytes (where TDM data can occupy 8, 16, 24, 32, or 40 payload bytes), and the remaining 8 bytes are devoted to AAL5 overhead. Every cell in a CBR-AAL5 VC is an end-of-frame cell, as identified by the LSB of the PTI field in the cell header being set. In addition, each cell contains a CPCS-UU byte and a CPI byte (both unused here), two length bytes and four CRC bytes (all inserted by the MT90500). The MT90500 supports TDM trunking over AAL5, for n = 1, 8, 16, 24, 32, or 40. For n = 1, the MT90500 meets the cell format in the ATM Forum standard AF-VTOA-0083.000.

4.3.2 TX_SAR Process

Figure 19 at the end of this section gives an overview of the processes explained below.

4.3.2.1 Transmit Event Schedulers

As discussed in Section 4.1.3, a 64-byte Transmit Circular Buffer is maintained in external memory for each TDM channel whose data needs to be transmitted on the ATM link. Structures known as “transmit event schedulers” are used to tell the hardware when a cell needs to be assembled for transmission.

The three transmit event schedulers all have similar properties and individual configuration registers. Each transmit scheduler is divided into a programmable number of “frames”. The circuitry operates to constrain each frame to last an average of 125 µs, which is the time required for 1 byte to be received / transmitted on each TDM channel. Within each frame 8, 16, or 32 VC Pointers can be programmed to transmit cells.

When multiple schedulers are used simultaneously, one must assume that any frame in one scheduler can be superposed onto any frame in another scheduler. To limit cell delay variation, each frame (composed of events from one, two, or three schedulers) should contain no more than 45 VC Pointers (or transmission events) for 155 Mbps systems, and no more than 7 VC Pointers for 25 Mbps systems. For example, if three schedulers are programmed and each scheduler’s most-filled frame contains respectively 22, 8, and 28 VC Pointers, the worst case scenario is a frame with 58 cells, thus over the 45 VC Pointers per frame limit for 155 Mbps. This type of situation must be avoided to minimize the cell delay variation resulting from an unbalanced or temporarily overloaded transmit scheduler. The TX_SAR will generate a fatal “SCHEDULE” error (see TX_SAR Status Register at 2002h) if more than 8 consecutive frames contain more than 7 (25 Mbps) or 45 (155 Mbps) VC Pointers. The same error may also occur when the TX_SAR is heavily loaded and other processes are using more bandwidth than they normally do. The RX_SAR and UTOPIA modules use the external memory’s bandwidth unevenly over time, depending on the rate at which cells arrive. They can cause “SCHEDULE” errors in the TX_SAR when the MT90500 is near its maximum load. This error is generated by the TX_SAR when it is at least 8 frames (1 ms) late.

To prevent cell delay variation, “SCHEDULE” errors, and TDM data unavailability, the software that configures the TX_SAR must use an efficient algorithm to fill the event schedulers. Events that send cells on the same VC must be evenly distributed in the event scheduler. The distance between two events associated with the same VC must be as constant as possible. For an 8-channel AAL1-SDT type cell (with a pointer byte sent in cell #0 of each sequence), the distance between two events must be 46.975/8 ~ 5.86 frames. Since this number must be an integer, the event spacing should be 6-6-6-5-6-6-6-5 frames. This regular transmission of cells is also important in limiting the CDV (Cell Delay Variation) of the transmitted cells.

Each programmable event scheduler is composed of a “base address”, a “short end”, a “long end”, a “long/short ratio” and a certain number of events per frame, as shown in Figure 15. This information is set in the TX_SAR registers located at addresses 2010h/2020h/2030h, 2012h/2022h/2032h, and 2014h/2024h/2034h.

The key to supporting different cell types is to have a programmable short and long end for each scheduler. For AAL1-SDT type cells, the scheduler ends at frame 45 for P-Type cells (short end) and at frame 46 for non P-Type cells (long end). The ratio between the long and short end can be programmed to either 1 (to generate P-Type cells every even-numbered cell), 3 (to generate P-Type cells every other even-numbered cell), or 7 (to generate P-Type cells once in every 8-cell sequence). The PSEL field in the Transmit Control Structure (Figure 16) must represent the long/short ratio in the event scheduler, except in the case of partially-filled cells. For a VC which is to carry partially filled cells, the long/short ratio is set to 0.

When the long/short ratio is equal to 0, the scheduler always counts to the long end before returning to frame 0. This mode is used for CBR-AAL0, CBR-AAL5, pointerless AAL1 Structured Data Transfer, and partially-filled cell formats, since the number of CBR payload bytes in these cells is constant (regardless of the value of the PSEL field). For a partially filled P-type cell (i.e. containing an AAL1 pointer-byte) one less pad byte is inserted after the TDM data than for a partially filled cell without a pointer byte. The event scheduler can be truncated down to as few frames as necessary to support the desired partially-filled cell length. On the other hand, the event scheduler can also be enlarged so that its length is an integer number which is a multiple of all the partial length formats that need to be supported. For example a scheduler of length 96 will support the following cell fill sizes: 1, 2, 3, 4, 6, 8, 12, 16, 24, 32, and 48. For specific examples regarding scheduler configuration, please refer to the MT90500 Programmers’ Manual.

When the MT90500 is used to transmit CBR-AAL5 cells, additional register programming is required to properly initialize the TX_SAR and the schedulers to send cells containing 32-bit CRCs. Regardless of which

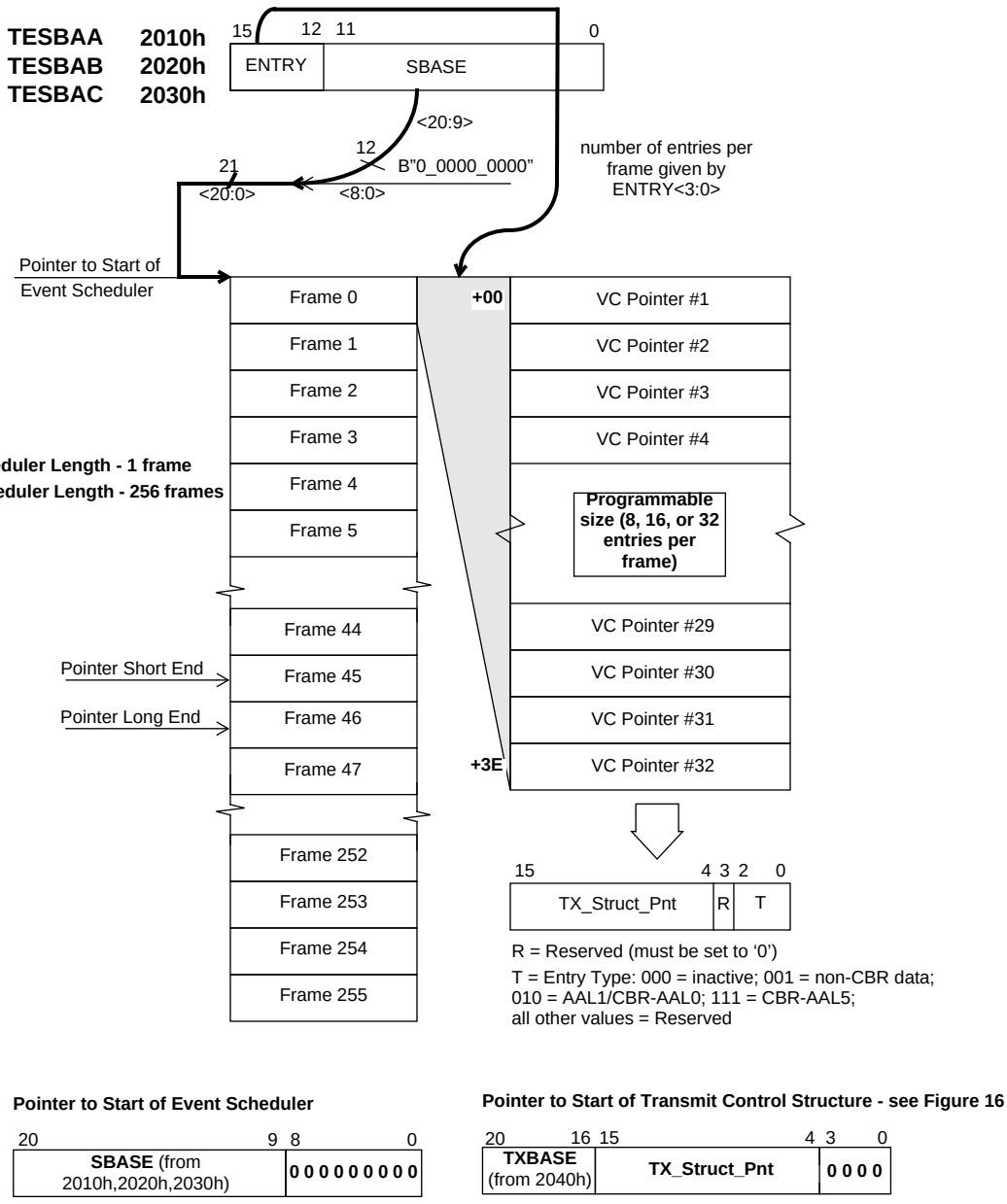


Figure 15 - Transmit Event Scheduler

scheduler(s) is (are) to be used for transmission of the ATM cells, the following initialization settings must be made:

- TX_SAR End Ratio Register - Scheduler A at 0x2014: set bits<7:6> = "01".
- TX_SAR End Ratio Register - Scheduler B at 0x2024: set bits<7:6> = "10"
- TX_SAR End Ratio Register - Scheduler C at 0x2034: set bits<7:6> = "11"

4.3.2.2 Transmit Control Structures

Within each frame within a transmit event scheduler 8, 16, or 32 VC Pointers can be programmed. Each entry represents a request to the hardware to generate a cell on that VC. An entry can be active or not, depending on the T bits located in the three LSBs of the entry word. An inactive entry is skipped. An active entry either tells the hardware to transmit the next non-CBR data cell held in the Transmit Data Cell FIFO in the external

memory (as explained in Section 4.3.3), or to transmit a CBR cell characterized by the Transmit Control Structure at the address pointed to by “TX_Struct_Pnt”. This latter process will be outlined in this section.

Once an active CBR VC Pointer is found in the event scheduler, the TX_SAR reads the structure (Figure 16 for CBR-AAL0 and AAL1 type cells, Figure 17 for CBR-AAL5 type cells) and may either send a cell or not. The ‘A’ bit in the structure indicates if the structure is active (an inactive structure will never generate a cell). When opening a VC, this three step procedure must always be followed: first, the software must write the Transmit Control Structure into the memory and clear both the ‘A’ and ‘S’ bits in that structure; second, all events pointing to the structure must be written in the event scheduler; finally, the ‘A’ bit must be set by the software. This procedure forces the hardware to ignore all events pointing to a structure until its ‘A’ bit is set. When the ‘A’ bit is set, all scheduler events for this VC immediately become active and the transmission process for this VC is enabled. Please refer to the MT90500 Programmers’ Manual, for detailed information on setting up a VC for the TDM to ATM Transmit Process.

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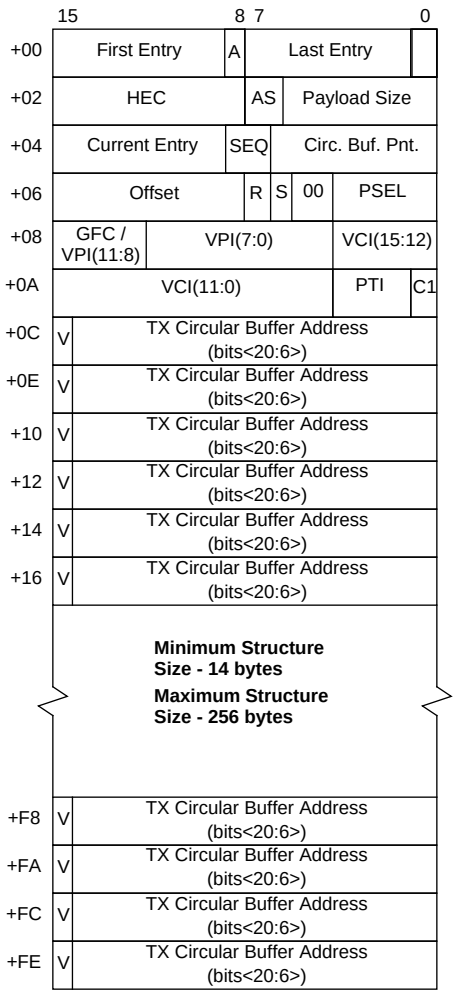


First Entry: indicates location of the first TX Circular Buffer Address within the Transmit Control Structure (lower bits are always 110).

A: Structure Active bit. '0' = inactive; '1' = active.

Last Entry: indicates where last TX Circular Buffer Address is located within the Transmit Control Structure.

HEC: HEC value (optional).

AS: AAL Type. "00"= CBR-AAL0/AAL5; "01"=Reserved; "10"=AAL1; "11"=Reserved

Payload Size: Indicates the number of payload bytes within an ATM cell. Full cell = 2Fh. Partially-filled cells = 03h to 2Eh.

Current Entry: indicates location of the current Transmit Circular Buffer. Must be initialized to First Entry value and is incremented by hardware.

SEQ: Indicates AAL1 sequence number. Possible sequence values are "000" to "111". Must be initialized by software to "000".

Circ. Buf. Pnt: This field must be initialized by software to initial offset required between TX_SAR Read Pointer and TDM Circular Buffer Write Pointer.

Offset: Offset value between the TDM Circular Buffer Write Pointer and the TX_SAR Read Pointer is stored in this field. Should be set to initial value of '0'.

R: Reserved (set to '0').

S: Structure Initialized. '0' = uninitialized; '1' = initialized. Must be set as '0' by S/W.

PSEL: P-Byte Selection. '0' for pointerless AAL1 Structured Data Transfer and CBR-AAL0; '8' for standardized SDT (see text for more details).

GFC: Cell Header GFC field (UNI).

VPI: Cell Header VPI field.

VCI: Cell Header VCI field.

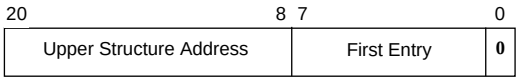
PTI: Cell Header PTI field. LSB of field, when set to '1', indicates OAM-type cell.

C1: Cell Header CLP bit.

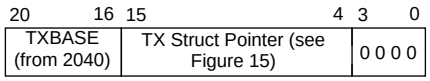
V: TX Circular Buffer Valid Bit. '0' = invalid entry; '1' = valid TX Circular Buffer address.

TX Circular Buffer Address: This is the upper part of the address that points to a Transmit Circular Buffer (bits 20:6). The buffer must be located relative to the TX Circular Buffer Base Address (TXCBBASE) set in register 6044h.

Pointer to First TX Circular Buffer Entry

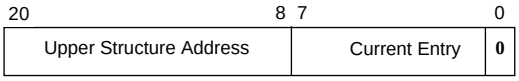


Pointer to Start of Transmit Control Structure

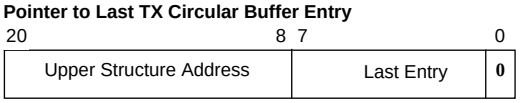


Note: Transmit Control Structures must start on 16-byte boundaries and **cannot** overlap 256-byte boundaries.

Pointer to Current TX Circular Buffer Entry

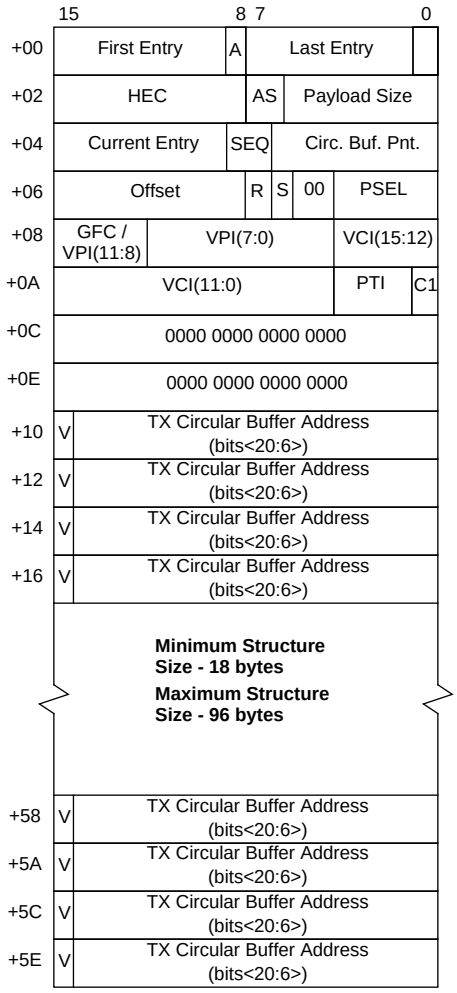


Pointer to Last TX Circular Buffer Entry



Note: Upper Structure Address is obtained from the upper 13 bits (i.e. bits<20:8>) of the Pointer to Start of Transmit Control Structure.

Figure 16 - Transmit Control Structure Format (AAL1 & CBR-AAL0)



Special Notes:

First Entry: indicates location of the first TX Circular Buffer Address within the Transmit Control Structure (lower bits are always 1000). **Note difference between first entry location in CBR-AAL5 Transmit Control Structure and AAL1/CBR-AAL0 Transmit Control Structure.**

AS: AAL Type. “00”= CBR-AAL5 (AAL5 cells are a special case of AAL0).

PSEL: P-Byte Selection. “0000” for CBR-AAL5.

PTI: LSB of field must be set to ‘1’ to identify this as a CBR-AAL5 type cell.

Figure 17 - Transmit Control Structure Format (CBR-AAL5)

If the structure has never been updated by the hardware, the “Circ. Buf. Pnt” field must indicate “how old” (in terms of 125µs TDM frames) the first byte in the first cell should be. For instance, if a cell contains 47 bytes, and the age of the first byte to be sent is 46, the last byte to be sent in the cell will have an age of -1 (i.e. it hasn’t arrived at the MT90500 yet). Thus, in the case of a single channel AAL1-SDT VC, the software must initialize the value of the Circ. Buf. Pnt. to at least 47, ensuring that at least 47 bytes are available for cell assembly when the scheduler is ready to transmit an event. This will also ensure that the most recent 47 bytes of data are sent. A value greater than 56, however, is not recommended because the oldest data to be sent in a cell may be overwritten by the TDM module and replaced by new data. A value of 51 to 56 is recommended for any single channel AAL1 or CBR-AAL0 fully-filled cell. When using hyper-channels or partially-filled cells, much lower values should be written in this field, thus reducing transmission delay. The following equations (used to calculate the initial “Circ. Buf. Pnt.” to be written by the software) are valid for most cell types:

AAL1 SDT-type Cells: Circ. Buf. Pointer = ROUNDUP ((max. # of payload bytes per cell / # of channels per VC) * ROUNDUP (# of channels per VC / min. # of payload bytes per cell * 4)) + 5

All other cells: Circ. Buf. Pointer = ROUNDUP ((max. # of payload bytes per cell / # of channels per VC) * ROUNDUP (# of channels per VC / min. # of payload bytes per cell * 4)) + 4

The “Offset” field is used by internal hardware to verify the offset between the TDM Circular Buffer Write Pointer and the TX_SAR Read Pointer (which is stored in Circ. Buf. Pnt. in the Transmit Control Structure, once the structure becomes active). Offset should be initialized to “00h”.

All Transmit Control Structures must begin on 16-byte boundaries, and may not overlap 256-byte boundaries. Any structure that overlaps a 256-byte boundary will cause unpredictable SAR behaviour. The “First Entry”,

"Current Entry", and "Last Entry" fields are pointers that must be set relative to the beginning of the particular Transmit Control Structure. The First Entry field represents the location of the first TX Circular Buffer Address within a Transmit Control Structure. This 7-bit field represents the 8 LSBs of the actual entry location divided by two (shifted right by one). When the Transmit Control Structure represents CBR-AAL0 or AAL1 type data, the lower three bits of the "First Entry" will always be "110" since the first entry is always 12 bytes away from the start of the Transmit Control Structure. When transmitting CBR-AAL5 type cells, the lower four bits of the "First Entry" will always be "1000" because the first TX Circular Buffer Address is located 16 bytes away from the start of the control structure. The "Current Entry" and "Last Entry" fields are programmed similarly, with "Current Entry" bearing the same address as "First Entry" when the structure is initialized by software. The programming of the First Entry and Last Entry fields for two examples can be seen below in Figure 18. Note that the Transmit Control Structure is not active until the A bit in the first byte of the structure is set HIGH.

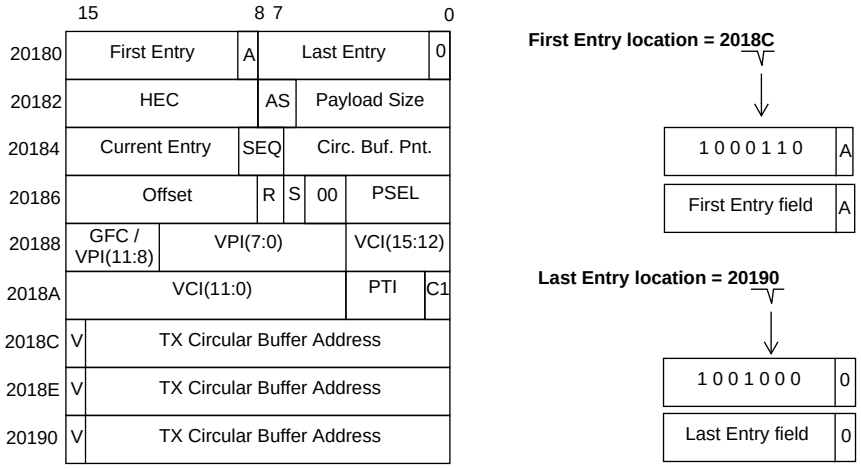


Figure 18 - a: Sample Three-Channel Transmit Control Structure (AAL1/CBR-AAL0)

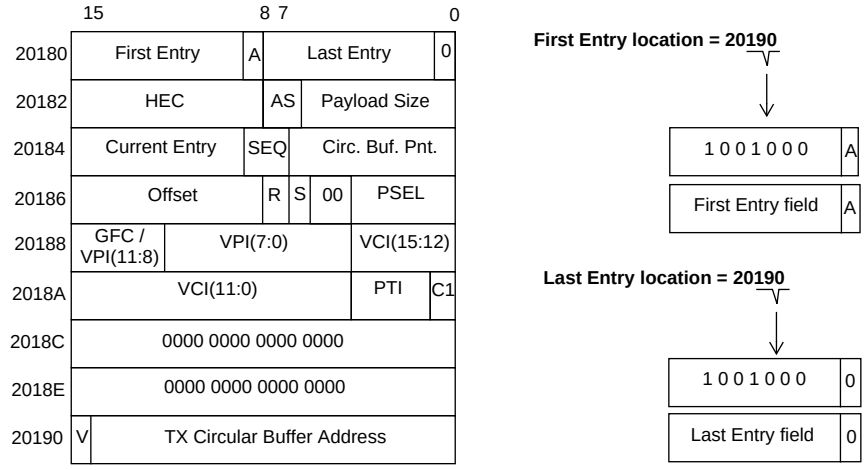


Figure 18 - b: Sample One-Channel Transmit Control Structure (CBR-AAL5)

The cell header portion of the Transmit Control Structure is passed directly to the UTOPIA bus without any modifications. Typically, the PHY device will calculate the HEC and over-write the HEC field in the Transmit Control Structure. However, in the case where the PHY device does not calculate the HEC field, the HEC byte may be calculated by the CPU, and written into the HEC field of the Transmit Control Structure.

The AS field indicates to the TX_SAR if the VC is a CBR-AAL0/AAL5 or AAL1 VC.

The "payload-size" field in the Transmit Control Structure indicates the number of TDM bytes carried in an ATM cell. For a fully-loaded cell of AAL1 or CBR-AAL0, the payload-size field must be set to a value of 2Fh (decimal

47) which represents a full payload for CBR-AAL0 (48 TDM bytes), pointerless AAL1 Structured Data Transfer (47 TDM bytes plus 1 AAL1 byte), and AAL1-SDT (47 TDM bytes plus 1 AAL1 byte, or 46 TDM bytes plus 1 AAL1 byte plus 1 pointer byte). For a fully-loaded cell of CBR-AAL5, the payload-size field must be set to a value of 27h (decimal 39) which represents a full payload for CBR-AAL5 (40 TDM bytes). For partially-filled cells, the payload-size field may be set to a value ranging from 03h to 2Eh. Note that these values represent different numbers of payload bytes, depending on the type of data structuring that is being used. For example, to represent a fill of 32 TDM bytes in each CBR-AAL0 or CBR-AAL5 cell, the user should set a payload-size of 1Fh. However, in order to ensure that each AAL1 cell (SDT or pointerless Structured Data Transfer format) contains 32 TDM bytes, the payload-size must be set to 20h. Similarly, while a payload-size of 7h indicates that the transmitted CBR-AAL0 or CBR-AAL5 cells contain 8 bytes of TDM data a payload-size of 8h is required to ensure a fill of 8 TDM bytes in each cell transmitted using AAL1-SDT or pointerless AAL1 Structured Data Transfer. In general, the payload-size field should be set to the expected number of TDM bytes when transmitting AAL1-type cells, and it should be set to one less than the expected number of TDM bytes when transmitting CBR-AAL0 and CBR-AAL5 cells. As well, it should be noted that 2Eh (decimal 46) is an illegal value for AAL1-SDT.

The PSEL nibble is used to denote the cell(s) within an 8-cell sequence in which the pointer byte (P-byte) is to be sent. When using pointerless AAL1 Structured Data Transfer, no pointer cells are ever sent, and the PSEL nibble must be initialized to 0h. With SDT, pointers may be sent in cells 0, 2, 4, or 6 of a sequence. The MT90500 can support both standardized and proprietary SDT formats. In order to meet ITU-T I.363.1, a structure (i.e. a specific VC) must be composed of no more than 96 channels, and the P-byte must be sent in the first (i.e. sequence number = 0) cell of each 8-cell cycle. Thus the PSEL field must be set to 1000 (the PSEL bits are one-hot bits which represent cells with sequence numbers 0, 2, 4, and 6, respectively - see Table 10 below for an explanation of bit operation). The MT90500 also supports proprietary pointer transmissions in which a P-byte is sent every 4 cells (PSEL = A hex) or every other cell (PSEL = F hex). Using these proprietary methods, up to 122 channels can be sent on a particular VC, but this is only possible if the receiving chip can handle the extra P-bytes during a cycle.

Table 10 - Effect of PSEL Field on P-byte Generation

	Sequence # 0	**Sequence # 2**	**Sequence # 4**	**Sequence #6**	**Applicable Standards**
0000	No pointers are sent.				**ANSI and ITU-T** - AAL0, AAL5, pointerless AAL1 Structured Data Transfer, and partially-filled cells
1000	Pointer sent.	-	-	-	**ANSI and ITU-T** - AAL1-SDT
1010	Pointer sent	-	Pointer sent	-	**ANSI** - AAL1-SDT
1111	Pointer sent	Pointer sent	Pointer sent	Pointer sent	**ANSI** - AAL1- SDT

Each “TX Circular Buffer Address” appended to the end of the structure points to a 64-byte circular buffer in external memory.

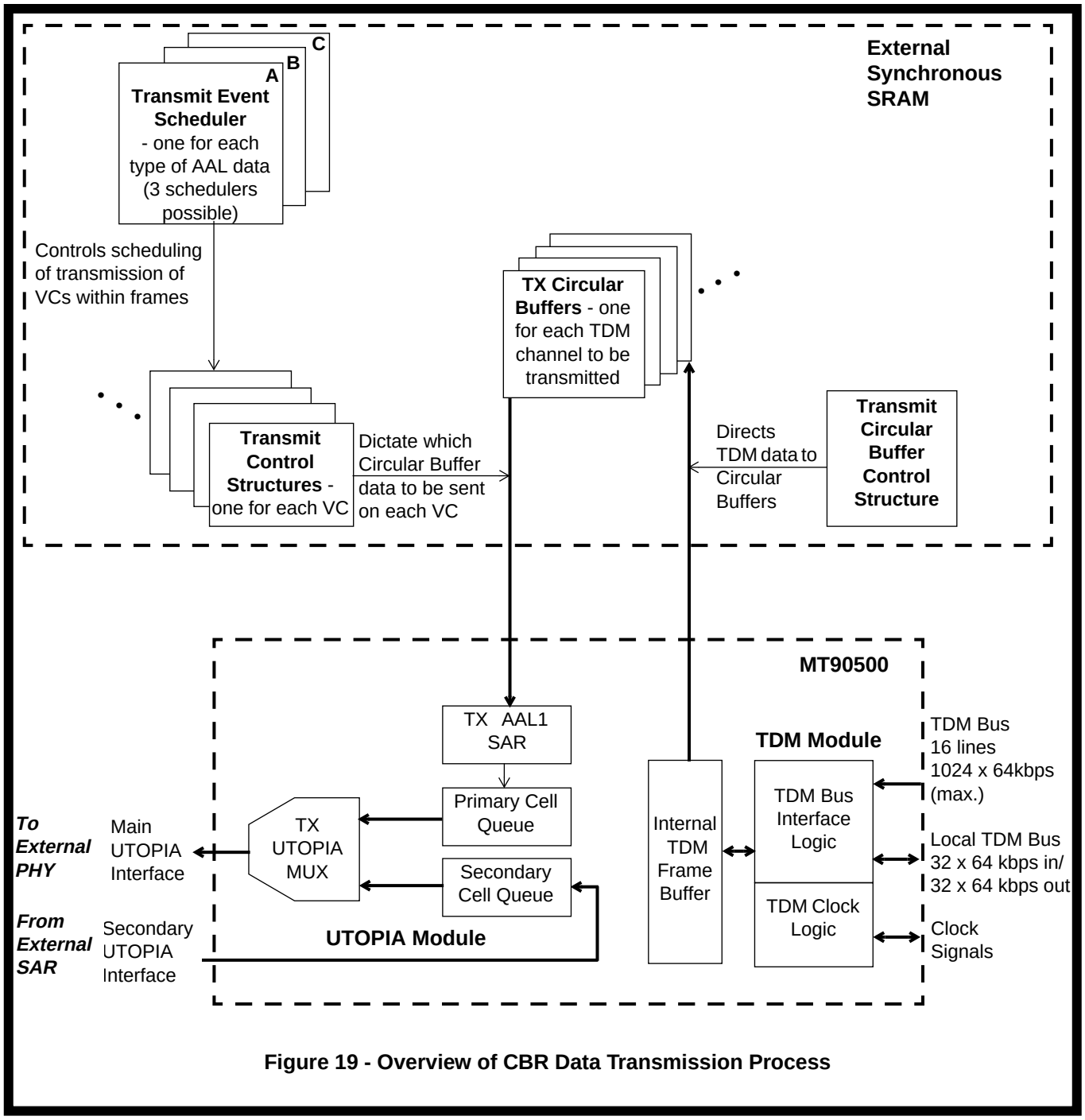
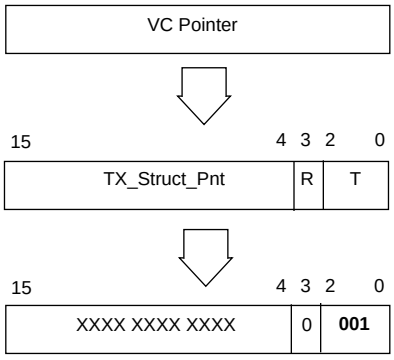


Figure 19 - Overview of CBR Data Transmission Process

4.3.3 Non-CBR Data Cell Transmission Capability

The TX_SAR also has the ability to transmit CPU-written non-CBR data cells directly from a user-defined FIFO in external memory (the Transmit Data Cell FIFO) to the UTOPIA module. Non-CBR data cells include OAM cells, other signalling cells, and AAL5 cells containing CPU data. Once the CPU writes the complete cell into the Transmit Data Cell FIFO, the UTOPIA module then treats these non-CBR data cells the same as the normal CBR cells. All 53 bytes of the non-CBR data cells are written by the microprocessor into the FIFO in 64-byte long structures located on 64-byte boundaries (see Figure 21). There are 16, 32, 64 or 128 of these structures contained in the circular FIFO, mapped in the external memory at the address determined by the Transmit Data Cell FIFO Base Address Register (register 2050h). This FIFO must not overlap an 8-Kbyte boundary. If the FIFO does overlap an 8K boundary, some or all of the non-CBR cells sent by the TX_SAR will be corrupted.

There are two ways to control transmission of non-CBR data cells: by scheduler, or by AUTODATA. The scheduler method requires mapping data cell events into one of the transmission schedulers being used. This is done by writing “001” in the Entry Type section of the VC Pointer entry, as shown in Figure 20.



R = Reserved (must be set to ‘0’)
T = Entry Type (000 = undefined; 001 = non-CBR data; 010 = AAL1/CBR-AAL0; 111 = CBR-AAL5; all others: Reserved)

Figure 20 - VC Pointer For Scheduler-Controlled Non-CBR Data Cell

In this case, when the scheduler hits the frame within which this entry is contained, it will read the next valid data cell from the Transmit Data Cell FIFO and transmit it. Because non-CBR cell transmission does not required the use of Transmit Control Structures, the TX_Struct_Pnt field in the VC Pointer is not used and thus its value is irrelevant. Note that using the scheduler(s) to control non-CBR data transmission results in regularly spaced non-CBR data cells, as specified in the scheduler entries.

The other possibility for controlling transmission of non-CBR data cells is by using the AUTODATA bit in the TX_SAR Control Register at 2000h. While that bit is HIGH, once the TX_SAR has completed its assigned cells for a certain quad frame (or frame) and is waiting for its next pulse (i.e. the TX_SAR is idle), the MT90500 will automatically transmit data cells, provided that data cells are available in the Transmit Data Cell FIFO. This process will end as soon as the next pulse is detected (**Note:** The non-CBR cell being treated at that time will be completed before the TX_SAR returns to CBR cell assembly).

Both these cases require the microprocessor to write the full non-CBR data cell into the Transmit Data Cell FIFO, and then to write the new (incremented) value of the Transmit Data Cell FIFO Write Pointer (address 2052h). Non-CBR data cells will only be sent if the Transmit Data Cell FIFO Write Pointer and the Transmit Data Cell FIFO Read Pointer (address 2054h) indicate that there are valid cells contained in the FIFO. When the pointers are not equal, the TX_SAR goes to the appropriate address indicated by the Transmit Data Cell FIFO Base Address Register (address 2050h) and reads the non-CBR data cell. Note that although the FIFO read pointer will be automatically adjusted to fit the Transmit Data Cell FIFO size (for example, if the FIFO size is 32 cells, when the read pointer is 31 and a cell is read, it will wrap around to 0), that is not true of the write pointer. Therefore, if the FIFO write pointer is set to 128, non-CBR cells will *always* be considered valid.

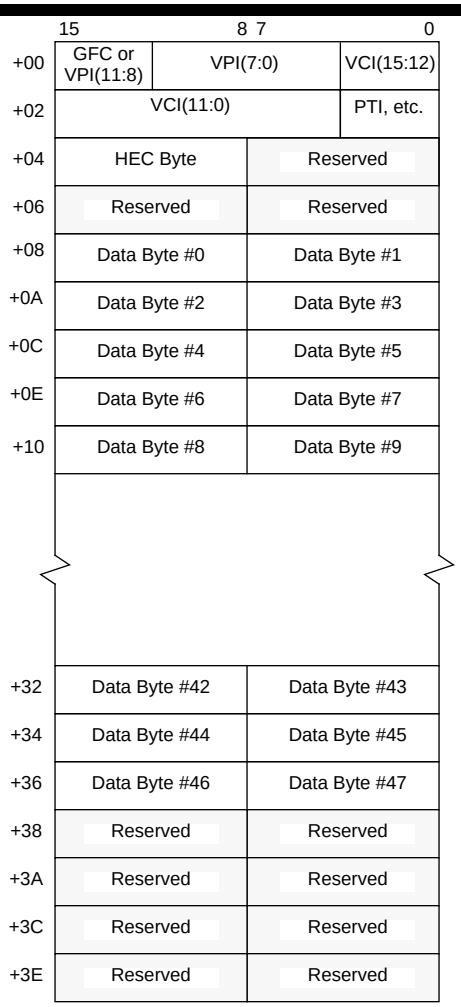


Figure 21 - Transmit Non-CBR Data Cell Structure Format

4.4 The RX_SAR Module

Figure 30 at the end of this section gives an overview of the processes explained below.

4.4.1 RX_SAR Overview

The RX_SAR block performs cell identification and reassembly functions on data moving from the Primary UTOPIA Port (refer to Section 4.5) toward the TDM interface. The RX_SAR module receives cells from the UTOPIA module, which has the capability of identifying cells as either CBR cells or non-CBR data cells. When non-CBR data cells are received by the UTOPIA module, they are stored in a multi-cell circular buffer located in external memory. When CBR cells are detected (AAL1, CBR-AAL5 or CBR-AAL0), they are processed and the payload is extracted and stored in time slot-related circular buffers, the size of which can be individually programmed by software on a per-VC basis.

The RX_SAR block supports AAL1-SDT, pointerless AAL1 structured data transfer (for ITU I.363.1 voiceband signal transport) and AAL0 cell formats. CBR-AAL5 cells are treated as partially-filled AAL0. Single or multiple (up to 122) TDM channels are supported per Virtual Circuit (specific VPI/VCI). On the receive side, the MT90500 RX_SAR block has the ability to receive and process up to 1024 Virtual Circuits simultaneously (and up to 1024 TDM channels at 64 kbps), resulting in a total of about 74 Mbps of bandwidth on the receive side. If 1024 TDM channels are used for full-duplex connections such as phone calls, the bandwidth will be ~74 Mbps per direction.

The amount of external memory required for the handling of receive VCs is variable and is defined by the user. The external memory requirements to support the RX_SAR are scalable and depend mainly on the number of TDM channels that need to be received on the ATM link and the size of the receive circular buffer required to compensate for latency and CDV (cell delay variation). As an example, the reception of 1024 simultaneous Virtual Circuits, each representing a 64 kbps channel, each with a 128 ms buffer, requires external memory capacity exceeding 1024 Kbytes (SRAM).

The RX_SAR module has no interface to the external pins. It has internal connections to the External Memory Controller, the UTOPIA module, and the Microprocessor Interface. It also receives synchronization signals from the TDM module. No fatal errors can be generated by the RX_SAR. Most of the registers associated with it are targeted at network statistics and error monitoring.

4.4.2 RX_SAR Process

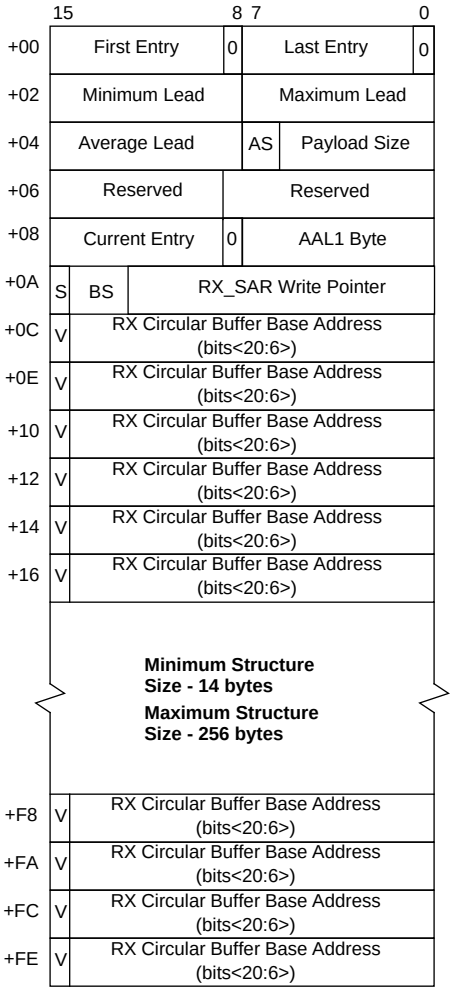
As explained in Section 4.5, detailing the operation of the UTOPIA module, cells received over the ATM link that are intended for the RX_SAR are tagged and forwarded to the RX_SAR module. For the traffic tagged as CBR, the RX_SAR then uses control information in the RX_SAR Control Structures to extract the payload data from the received cell and store it into TDM channel RX Circular Buffers located in external memory. For the traffic tagged as non-CBR data, the RX_SAR simply stores the whole cell, which is considered to be a raw AAL0 cell, in a circular FIFO located at the address specified by the Receive Data Cell FIFO Base Address Register (4020h). This will be explained further in Section 4.5.4. In addition, timing reference cells (which may carry CBR traffic or non-CBR data) can also be received on the ATM side of the MT90500. As outlined more fully in Section 4.5.3, the reception of these cells results in the generation of timing pulses used in Adaptive Clock Recovery.

For each VC assigned to CBR traffic in reception, an RX_SAR Control Structure has to be set up and maintained in external memory, as explained below.

4.4.2.1 RX_SAR Control Structures

The RX_SAR Control Structure is quite similar to the Transmit Control Structure shown in Figure 16, but it has added cell delay variation control fields (as seen in Figure 22). The “First Entry”, “Current Entry”, “Last Entry”, “AS”, “S”, “Payload Size”, “V”, and “RX Circular Buffer Base Address” fields all have the same properties as in the TX_SAR.

Three cell delay variation control fields must be initialized by the software: the “Minimum Lead”, “Maximum Lead” and “Average Lead”. Each of these fields is concatenated with “00” (i.e. multiplied by 4) to have a range from 0 to 1020. Before disassembling any cell, the RX_SAR verifies its write pointer’s validity with respect to the Maximum and Minimum Lead fields, as discussed in Section 4.4.2.2.



First Entry: Indicates location of the first RX Circular Buffer Base Address within the RX_SAR Control Structure.

Last Entry: Indicates where the last RX Circular Buffer Base Address is located within the RX_SAR Control Structure.

Minimum Lead: Indicates the minimum number of bytes that must always be valid in the RX Circular Buffer (to get the number of bytes, multiply Minimum Lead by four). Usually initialized to 01h.

Maximum Lead: Indicates the maximum number of bytes that may be valid in the RX Circular Buffer (to get the number of bytes, multiply Maximum Lead by four).

Average Lead: Indicates the average number of bytes that are valid in the RX Circular Buffer (to get the number of bytes, multiply Average Lead by four). Equal to (Minimum Lead + Maximum Lead) / 2.

AS: AAL Type. “00”= CBR-AAL0 & CBR-AAL5; “01”=Reserved; “10”=AAL1; “11”=Reserved

Payload Size: Indicates the number of payload bytes within an ATM cell. Full cell = 2Fh (48 bytes). Partially-filled cells = 03h to 2Eh.

Current Entry: Indicates location of the current Receive Circular Buffer. Must be initialized to First Entry value and is incremented by hardware (or realigned with arrival of pointer byte).

AAL1 Byte: Used by hardware to check for cell loss / misinsertion. Should be initialized to 00h.

S: Structure Initialized. ‘0’ = uninitialized; ‘1’ = initialized. Must be set as ‘0’ by S/W.

BS: Circular Buffer Size. “000” = 64 bytes; “001” = 128 bytes; “010” = 256 bytes; “011” = 512 bytes; “100” = 1024 bytes; other = reserved.

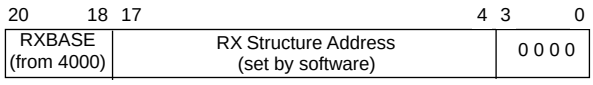
RX_SAR Write Pointer: When S bit is ‘0’, uninitialized; when S bit is ‘1’, indicates which byte in the RX Circular Buffer the hardware will write first with the data in the next cell.

V: Receive Circular Buffer Valid Bit. ‘0’ = not valid; ‘1’ = valid (write received cell data to a circular buffer).

RX Circular Buffer Base Address: This is the upper part (bits 20:6) of the address that points to a Receive Circular Buffer. **Note**: RX Circular Buffers **must** be located on boundaries corresponding to the size of the buffer (see Figure 7 on page 35 for clarification).

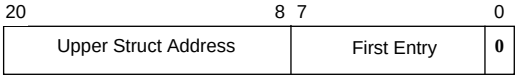
Reserved: Set to all zeroes.

Pointer to Start of RX_SAR Control Structure

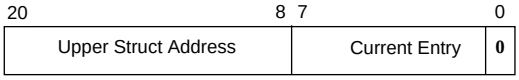


Note: RX_SAR Control Structures must start on 16-byte boundaries and **cannot** overlap 256-byte boundaries.

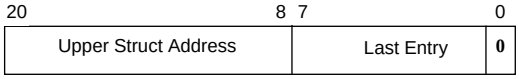
Pointer to First RX Circular Buffer Entry



Pointer to Current RX Circular Buffer Entry



Pointer to Last RX Circular Buffer Entry



Note: Upper Struct Address is obtained from the upper 13 bits (i.e. bits<20:8>) of the Pointer to Start of RX_SAR Control Structure.

Figure 22 - RX_SAR Control Structure

The AAL1 byte is used by hardware to check the cell sequence number and therefore provide cell loss / misinsertion detection. Before opening a VC, the user should write 00h into this field and then leave it for hardware control.

The “BS” field indicates the size of the Receive Circular Buffers. The valid size ranges from 64 to 1024 bytes and depends upon the amount of available memory and the cell delay variation (CDV) in the network. Note that

all channels arriving on the same VC must have the same CDV and therefore their RX Circular Buffers will all be the same size.

The “RX_SAR Write Pointer” is initialized to zero by software and used only by the hardware.

Unlike the Transmit Control Structures, there is no difference in the configuration of the RX_SAR Control Structures for the various cell types. In fact, the only thing which differentiates the control structures for different AALs is the AS field. In particular, this field is set to “00” for CBR-AAL0 and CBR-AAL5 cells (because CBR-AAL5 is really just a special case of CBR-AAL0), or “10” for AAL1.

As with the Transmit Control Structures, all RX_SAR Control Structures must start on 16-byte boundaries and must never cross 256-byte boundaries.

4.4.2.2 RX_SAR Overrun/Underrun Situations

The “First Entry” and “Last Entry” fields in the RX_SAR Control Structure point to the first and last RX Circular Buffer Base Address pointers in the RX_SAR Control Structure. The “Minimum Lead”, “Maximum Lead”, and “Average Lead” entries define the window within the circular buffer within which cell data can be received without generating an underrun or overrun condition. This window is defined relative to the TDM Circular Buffer Read Pointer, as described in Figure 23. Whenever data from a newly received cell is to be written to the Receive Circular Buffers, the location of the RX_SAR Write Pointer is checked against the Minimum and Maximum Lead Pointers.

Three 16-bit error counters and three error structure ID registers are available for network performance monitoring. When receiving a cell, any of the following errors can be detected: an overrun slip, an underrun slip, an AAL1 byte parity error, an AAL1 CRC error, a sequence number error, a P-byte parity error, or a P-byte out of range error. A counter and ID register are used to monitor each of the slip-type errors (3022h and 3020h for Underrun events; 3032h and 3030h for Overrun events). The other five types of errors share common counter (3012h) and event ID (3010h) registers. Five bits in the RX_SAR Control Register (3000h) allow the control software to choose which error events affect the count and ID registers. If more than one error count enable is active, the counter will add all occurrences of the various errors. The ID register points to the RX_SAR Control Structure which experienced the last recorded error. All of the errors should be self-explanatory, except for the P-byte out of range error. This error occurs when the P-byte’s value implies that a hyper-channel contains more channels than indicated by the RX_SAR Control Structure.

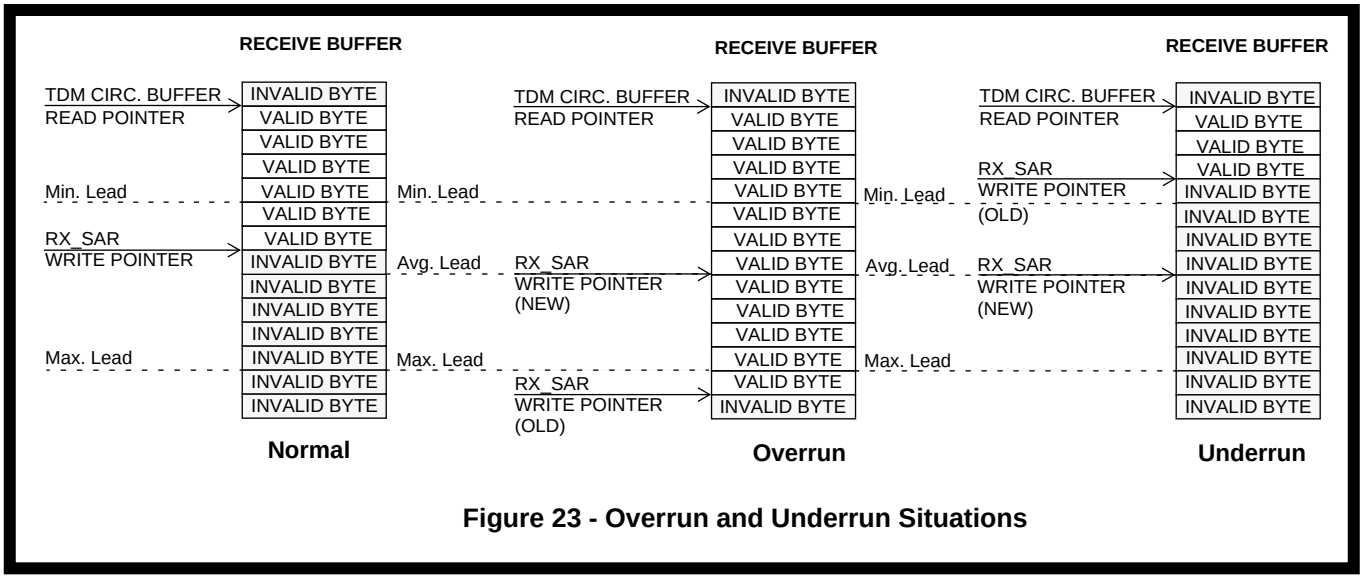


Figure 23 - Overrun and Underrun Situations

When a new cell is received, the hardware checks for the location of the RX_SAR Write Pointer, which indicates where the new cell should be written within the associated Receive Circular Buffer(s). The VALID bytes shown in the figure above indicate bytes which have been written by the RX_SAR and have yet to be read by the External Memory to TDM Data Output Process. Consequently, INVALID bytes represent those that have already been read or, in the case of start-up, have never been written. If the pointer falls within the window defined by the Min. Lead and Max. Lead parameters, the new data is written immediately following the old data.

If the RX_SAR Write Pointer falls after the Maximum Lead Pointer, an overrun condition is detected, and the new data is written starting at the location of the Average Lead Pointer. (Some addresses containing previously received, unread data bytes are overwritten.) If the RX_SAR Write Pointer falls before of the Minimum Lead Pointer, an underrun condition is detected, and the new data is written starting at the location of the Average Lead Pointer. (Some addresses containing already-read data bytes are “skipped” and left unwritten.) Figure 23 depicts the Write Pointer to Read Pointer comparison that occurs at cell receive time.

Data bytes which have been read by the TDM read process (External Memory to TDM Data Output Process in Section 4.1.4) are handled according to the programming of the External Memory to Internal Memory Control Structure. Depending on the value of the write-back disable bit for each individual TDM channel, bytes read out to the TDM bus will either be replaced by silence (FFh) or left unchanged. This has the effect that in the event of an underrun, either silence (FFh) will be read out of the “skipped” area, or the old data in the “skipped” area will be repeated on the TDM bus.

The TDM read process has its own TDM Read Underrun Error indication (see register 6000h) which works in parallel to that described above. The ninth bit of the external memory byte is used to indicate whether each byte has been previously transferred to the TDM bus. When the External Memory to TDM Data Output Process reads a byte which has already been transferred, an underrun condition is flagged (if enabled by that TDM channels entry in the External Memory to Internal Memory Control Structure). Since this TDM Read Underrun Error functions as each byte is read (and not just when a cell arrives, as the RX_SAR errors do) it is useful to indicate dropped VCs (no cells), and excessive CDV (late cells).

Registers are used to maintain statistics on the occurrence of underrun and overrun conditions. The last VC where an underrun or overrun condition was detected is also recorded in an event ID register.

Note: Care must be taken when assigning the Maximum Lead value for small circular buffers: when the Maximum Lead is too far from the TDM Read Pointer, the reception of a cell could write new data over the data being read by the TDM module. This error can occur if {(Maximum Lead) + (# of Bytes in Cell)} ≥ (Circular Buffer Size).

4.4.2.3 Lost Cell Handling

In the event of a lost cell, the MT90500 maintains bit count integrity through buffer-fill level monitoring, rather than through sequence number processing (ITU-T Rec. I.363.1 terminology). Sequence numbers are however monitored, and errors are reported (registers 3000h and 3002h). In the event of a single cell loss:

- RX_SAR Write Underrun will detect underrun if the CDV tolerance is depleted (3002h);
- TDM Read Underrun will detect underrun if Rx Circular Buffer is depleted (6002h);
- Sequence number error will be detected (3002h).

In the event of loss of multiple consecutive cells:

- RX_SAR may detect Write Underrun or Write Overrun (dependent on number of cells lost, and Rx circular buffer size);
- TDM Read Underrun will detect underrun if Rx Circular Buffer is depleted;
- Sequence number error will be detected.

In the event a VC gets disconnected:

- TDM Read Underrun will detect underrun (once Rx Circular Buffer is depleted).

Note that the operation of the TDM Read Underrun Error bit requires that the TDM Read Underrun Detection Enable bit in the External to Internal Memory Control Structure be asserted (for the particular TDM channel in question) and 9-bit (parity) memory is used (36-bit rather than 32 bit external memory). In the event of a cell loss not large enough to trigger one of the underrun alarms, the TDM data is read as normal from the Rx Circular Buffer. This will “jump” the data from the lost cell, similar to a frame slip in TDM switches. In the event of a TDM Read Underrun Error, the TDM output depends on the state of the External Memory to Internal Memory Control Structure write-back disable bit, as explained in Section 4.4.2.2.

4.5 UTOPIA Module

On the ATM transmit side, the MT90500 multiplexes ATM cells generated by the internal TX_SAR module with ATM cells coming from the Secondary UTOPIA Port. Cells coming from the Secondary UTOPIA Port may be generated by the optional external SAR device (e.g. AAL5 SAR) or another MT90500 device (see Figure 58, “UTOPIA Bus Interconnections for Two MT90500s and an AAL5 SAR,” on page 125 for an application example).

4.5.1 UTOPIA Overview

The UTOPIA module is used to daisy chain one or several SAR devices in order to use a single PHY device, as seen below in Figure 24.

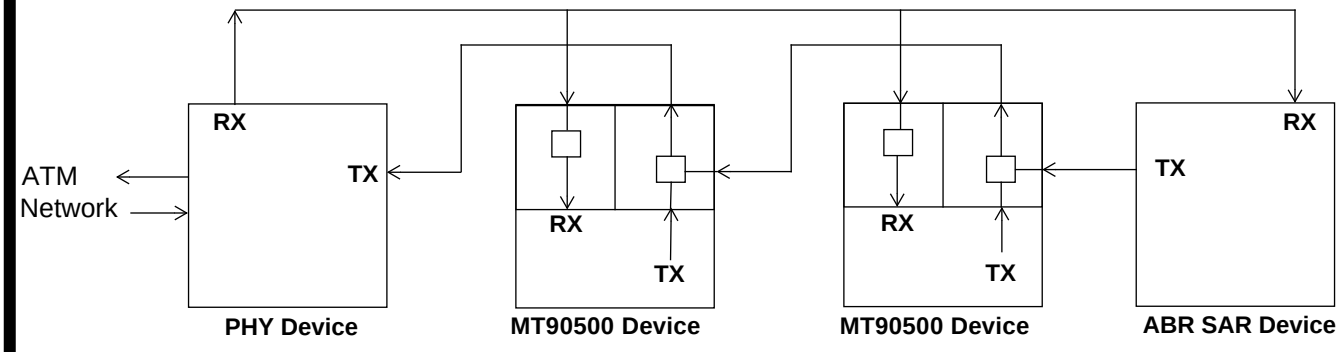


Figure 24 - MT90500 Daisy Chain Example

In the transmit direction, the Secondary UTOPIA Port of the MT90500 emulates a PHY, receiving cells from other SAR devices on the bus. The MT90500 then forwards these cells to the actual PHY using the Primary UTOPIA bus. The transmit portion of the UTOPIA module multiplexes the cell traffic from the Secondary UTOPIA bus with the cell traffic from the MT90500’s TX_SAR. A small internal FIFO is used to buffer up to four Secondary UTOPIA bus cells) and four TX_SAR cells. The TX_SAR and Secondary UTOPIA bus can have the same transmit priority, or the priority can be given to the TX_SAR (this is determined by the Round-Robin Priority bit in the UTOPIA Control Register at 4000h). No overruns are possible in the TX part of the UTOPIA interface since flow control (UTOPIA bus handshaking) is used.

On the receive side, the MT90500 passively taps the Receive UTOPIA bus. Since the Receive UTOPIA bus is multi-drop, cells may be received by more than one device. This can be used for redundant transfer of data or timing. Cells can be received at the maximum transfer rate of the bus (up to 25 MHz). When a cell is received, its header is analyzed: the cell is either ignored, or stored in the Primary Receive FIFO. (Ignored cells are assumed to be destined for another device on the Receive UTOPIA bus.) The Primary Receive FIFO is internal to the MT90500, and can contain 32 cells. If the internal Primary Receive FIFO is full, the received cell is discarded, so it is important to use a master clock rate (MCLK) fast enough for the application. Further details on the cell reception process are given in Section 4.5.3.

All cell transfers on both UTOPIA buses are performed using cell-level handshaking. See AF-PHY-0017 for more information regarding UTOPIA standards. For details on chaining UTOPIA devices, see the Applications section of this datasheet.

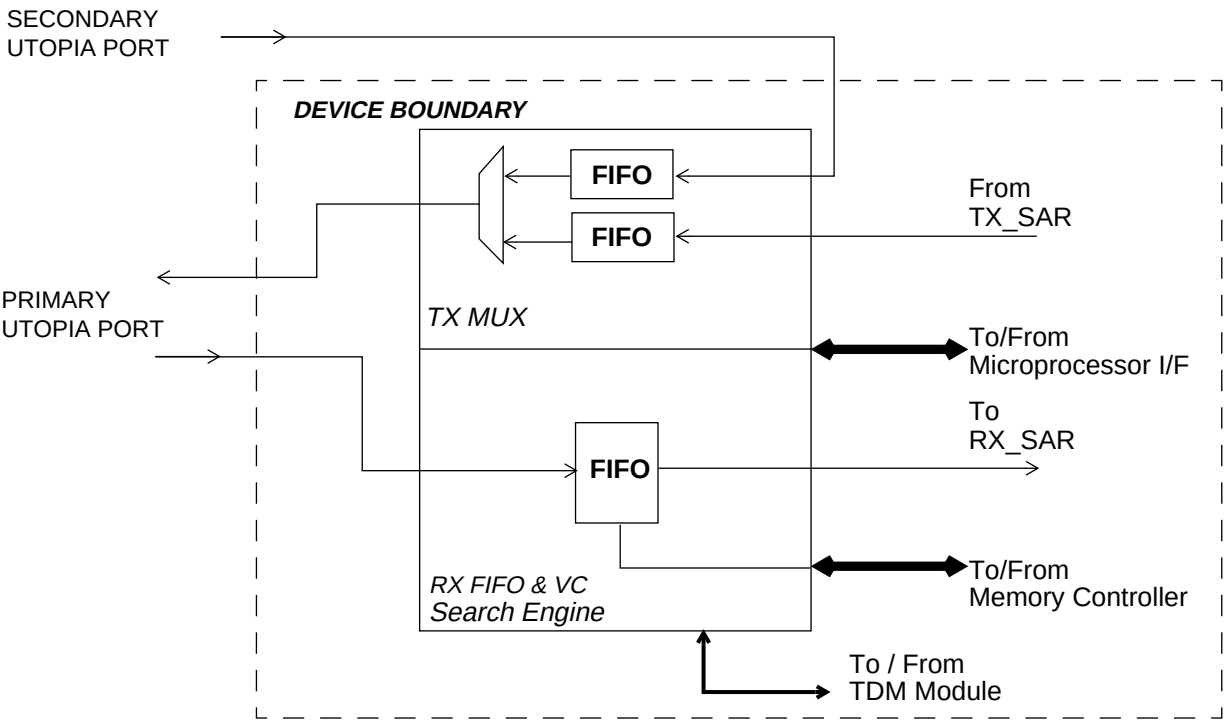


Figure 25 - Mux and Internal FIFO Sub-Module Block Diagram

4.5.2 Cell Transmission and Mux Process

The general block diagram of the Mux and internal FIFO sub-module is shown above. The Mux sub-module's operation is relatively straight-forward. It multiplexes onto the Primary Transmit UTOPIA Port cells generated by the TX_SAR with cells received from the optional external SAR device. A number of register bits found at address 4000h control the operation of the sub-module: a general enable (RXENA); an external SAR interface enable (STXENA); and a mux arbitration method (RRP, which gives priority to the TX_SAR or allocates priority in round-robin fashion).

4.5.3 Receive Cell Selection Process

The purpose of the Receive Cell Selection Process is to determine the routing of received ATM cells, which can include OAM cells, timing reference cells, CBR cells destined for the RX_SAR, and non-CBR data cells which will be routed to the Receive Data Cell FIFO. The steps involved in the Receive Cell Selection Process are detailed below and are outlined in the flow chart in Figure 26.

The Receive Cell Selection Process is as follows:

a) The most significant bit of the PTI field in the cell header is examined to determine if the cell is an OAM cell. If the received cell is an OAM cell, it is either sent to the 32-cell (2048-byte) internal Primary Receive FIFO, or discarded as determined by the OAM Routing Select bit, OAMSEL, in the UTOPIA Control Register at 4000h. OAM cells that are sent to this internal FIFO are then treated as non-CBR data cells and are eventually sent to the Receive Data Cell FIFO in external memory; see step (e). If the cell is not an OAM cell, step (b) is taken.

b) Non-OAM cells are then passed through the MT90500's timing filter mechanism. The VPI and VCI values of the incoming cell are compared to the values found within the VPI Timing Register (401Ah) and the VCI Timing Register (401Ch). If the VC of the received cell matches the Timing Registers, a timing pulse is sent to the Clock Recovery Module, along with the AAL1 byte of the cell header (this process is explained in detail in Section 4.6.1, "Adaptive Clock Recovery Sub-Module"). Regardless of whether the cell matches the timing filter or not, the cell is sent to step (c) for further processing.

c) The cell's VPI field (8 bits) is examined. A bit by bit comparison of the VPI is performed using the contents of both the VPI Match Register (4012h) and the VPI Mask Register (4014h). If a bit value in the VPI Mask Register is '0', no comparison is performed on the corresponding bit in the VPI Match Register (and the bit is automatically accepted). If a bit value in the VPI Mask Register is '1', the comparison result will only be true if the received VPI bit and the corresponding VPI Match Register bit are identical. The cell will only be processed further (i.e. proceed to step (d)) if each of the 8 bit comparisons produces true results. Otherwise, the cell will be discarded.

d) The cell's VCI field (16 bits) is then examined. A bit by bit comparison of the VCI is performed using the contents of both the VCI Match Register (4016h) and the VCI Mask Register (4018h). If a bit value in the VCI Mask Register is '0', no comparison is performed on the corresponding bit in the VCI Match Register. If a bit value in the VCI Mask Register is '1', the comparison result will only be true if the received VCI bit and the corresponding VCI Match Register bit match. Step (e) will only be executed if each and every one of the 16 bit comparisons produces true results. Otherwise, the cell will be discarded.

Note: The VPI/ VCI match and mask filter serves two important purposes. It can eliminate non-unique look-up-table entries (important as the look-up-table space is smaller than the entire VPI/VCI space of 16M addresses). It can also reduce the number of unnecessary look-up-table accesses (and unnecessary memory-access bandwidth) by eliminating cells with VPI/VCI not destined for the MT90500. The user is advised to set the VPI/ VCI match and mask filter as narrowly as practical for the application.

e) Any cell which passes through both the VPI and VCI match filtering will be placed in the 32-cell FIFO of the UTOPIA module. Cells are then read out by another internal process. As mentioned in step (a) above, OAM cells which are located in the Primary Receive Queue are automatically placed into the Receive Data Cell FIFO. On the other hand, non-OAM cells are passed to the lookup engine of the UTOPIA module, as explained in step (f).

(f) Within the look-up engine, the N least significant bits of the VCI and the M least significant bits of the VPI are concatenated together to form a 15-bit word. If M + N is smaller than 15, the missing most significant bits of the 15-bit word are zeroed. Two least significant zeroes are appended automatically (by H/W) to this word to form a 17-bit pointer aligned on a double-word boundary. **Note:** This is explained more fully in the register description for the VPI/VCI Concatenation Register at address 4010h. This pointer is added to the contents of the Look-up Table Base Address Register at address 401Eh to form a memory pointer into the VC Look-up Table, which is composed of 32-bit entries. The look-up engine then examines the "T" bits of each look-up table entry. These bits indicate the type of information being carried by a particular cell and therefore determine the final destination of the cell:

- "00" indicates an undefined cell type. In this case, the cell is either discarded or treated as a non-CBR data cell which is placed in the Receive Data Cell FIFO. This final cell routing is dependent on the setting of the UKSEL (Unknown Routing Select) bit in the UTOPIA Control Register at 4000h.
- "01" represents a non-CBR data cell. In this case, the cell is stored in a 64-byte long structure within the Receive Data Cell FIFO (see Figure 29).
- "10" indicates a CBR cell. In this case, the RX Structure Address in the look-up table (Figure 27), is used to access the RX_SAR Control Structure (see Figure 22 - RX_SAR Control Structure) to determine how to process the cell payload data.

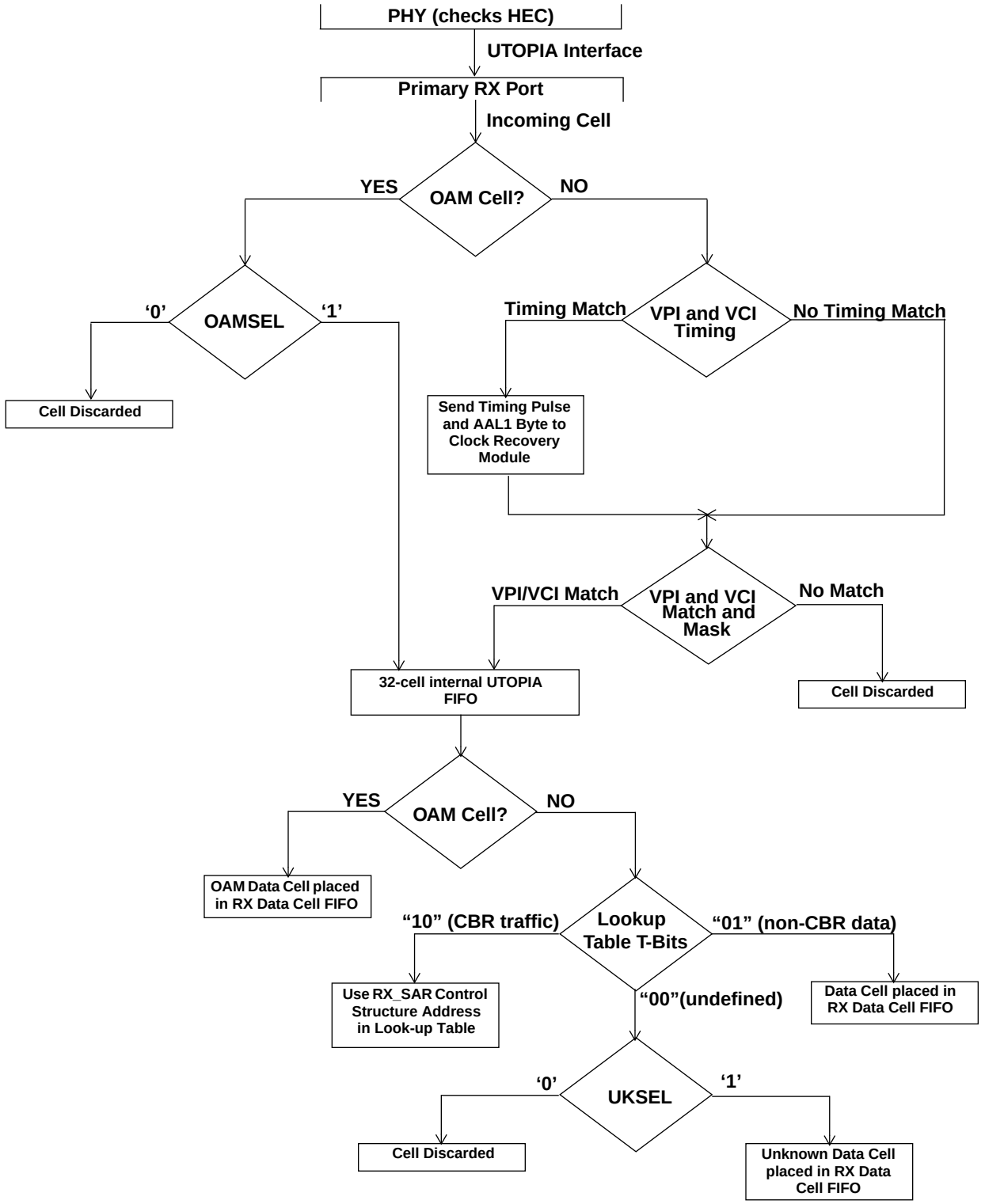


Figure 26 - Receive Cell Selection Process

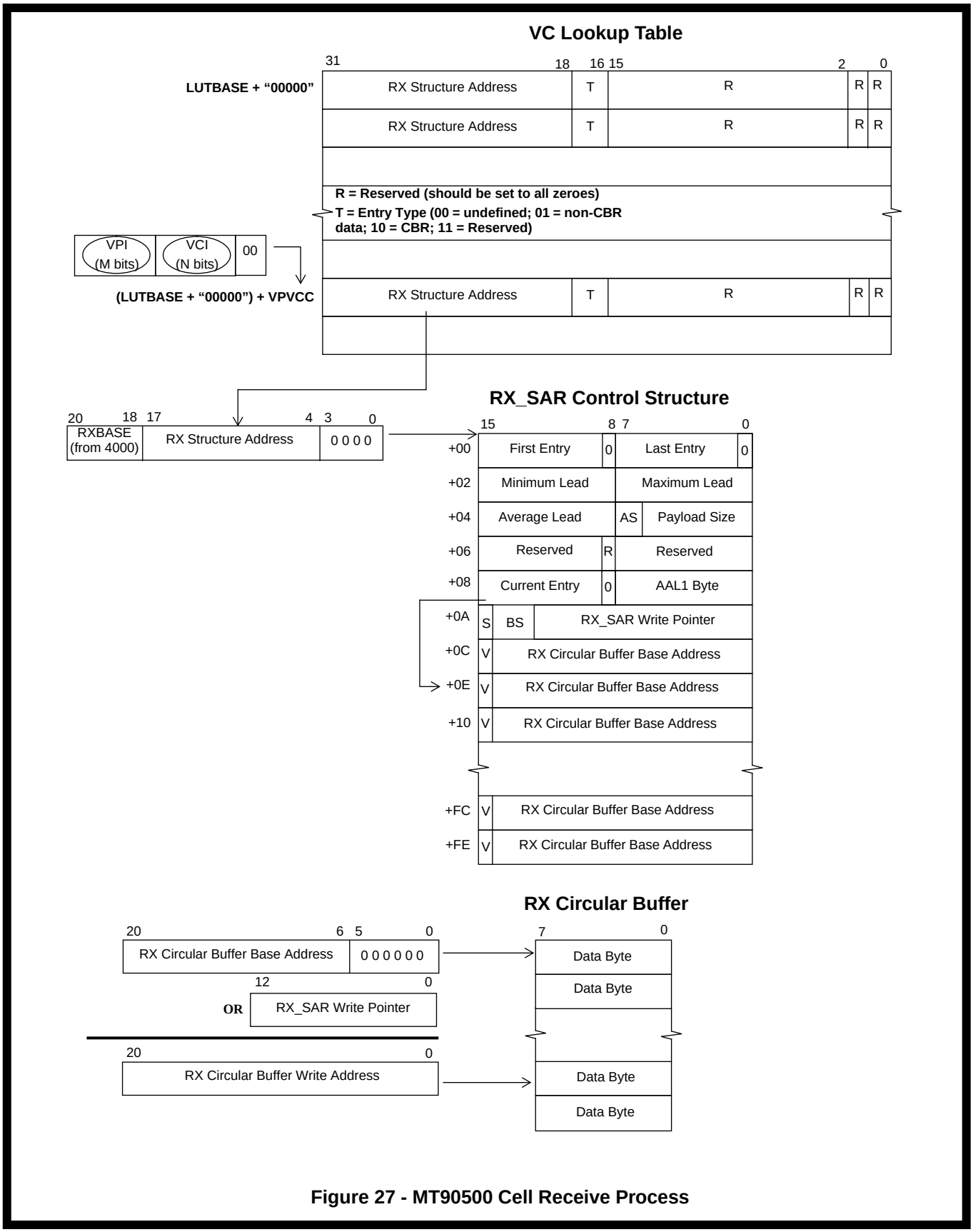


Figure 27 - MT90500 Cell Receive Process

4.5.4 Non-CBR Data Cell Reception Ability

As mentioned above, the MT90500 is capable of receiving non-CBR data cells as well as CBR cells. Non-CBR cells can be received on the UTOPIA bus and written into the user-defined Receive Data Cell FIFO in external memory, where they wait for the CPU to read them.

There are 3 ways for cells to be identified as data cells. First of all, OAM cells may be treated as non-CBR cells if the OAM Routing Select bit in the UTOPIA Control Register (address 4000h, bit<5>) is set to 1. Secondly, unknown cells may be considered as non-CBR cells if the Unknown Routing Select bit (bit<6> of the UTOPIA Control Register) is set to 1. Finally, normal cells whose VPI and VCI values correspond to those in the VPI and VCI Match Registers located at 4012h and 4016h respectively, can be tagged as data if their entry in the look-up table is associated with a non-CBR entry.

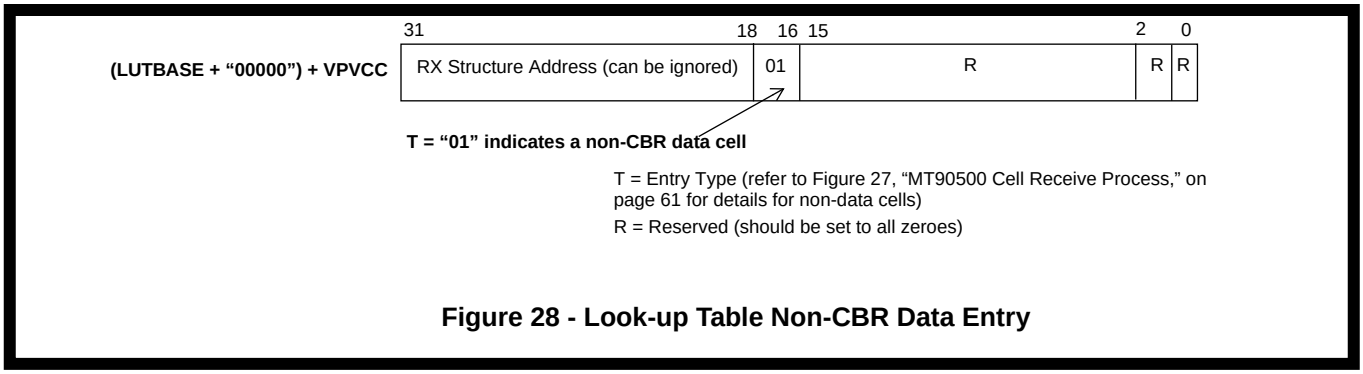


Figure 28 - Look-up Table Non-CBR Data Entry

To write into the Receive Data Cell FIFO, the chip will use the Receive Data Cell FIFO Base Address Register (address 4020h) and will write into the next available entry as tagged by the Receive Data Cell FIFO Write Pointer Register (address 4022h), regardless of the value in the RX Structure Address field of the look-up table entry. Once this is done, the write pointer will be incremented.

Finally, the CPU should read the data contained in the FIFO once the write pointer becomes greater than the read pointer. To do so, the CPU should access each of the 24 word entries corresponding to that cell (24 words * 2 bytes = 48 bytes, max. cell payload). Once it has completed its task, the read pointer should be incremented to ensure the hardware knows the cell has been read.

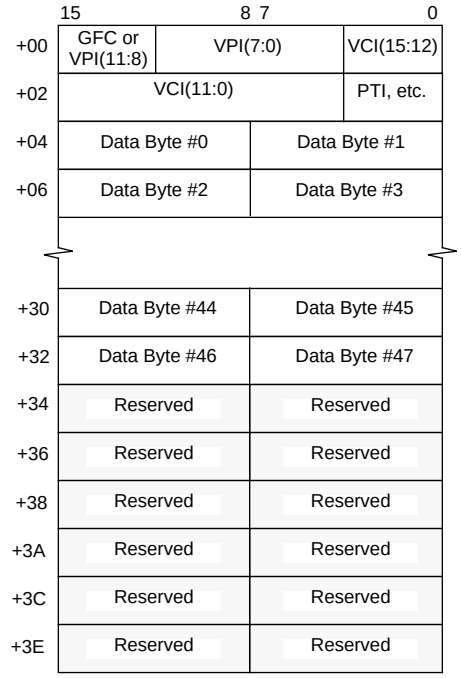


Figure 29 - Received Non-CBR Data Cell Internal Format

Should the CPU not read the appropriate data cells or should a huge concentration of non-CBR cells arrive consecutively on the Primary UTOPIA Port, a Receive Data Cell FIFO Overrun will occur. This error, indicated by bit<10> of the UTOPIA Status Register (address 4002h), indicates that the oldest data cell in the FIFO has been over-written due to lack of space for valid cells. Should this occur, the CPU will have to read the non-CBR cells faster or, conversely, the Receive Data Cell FIFO size should be increased.

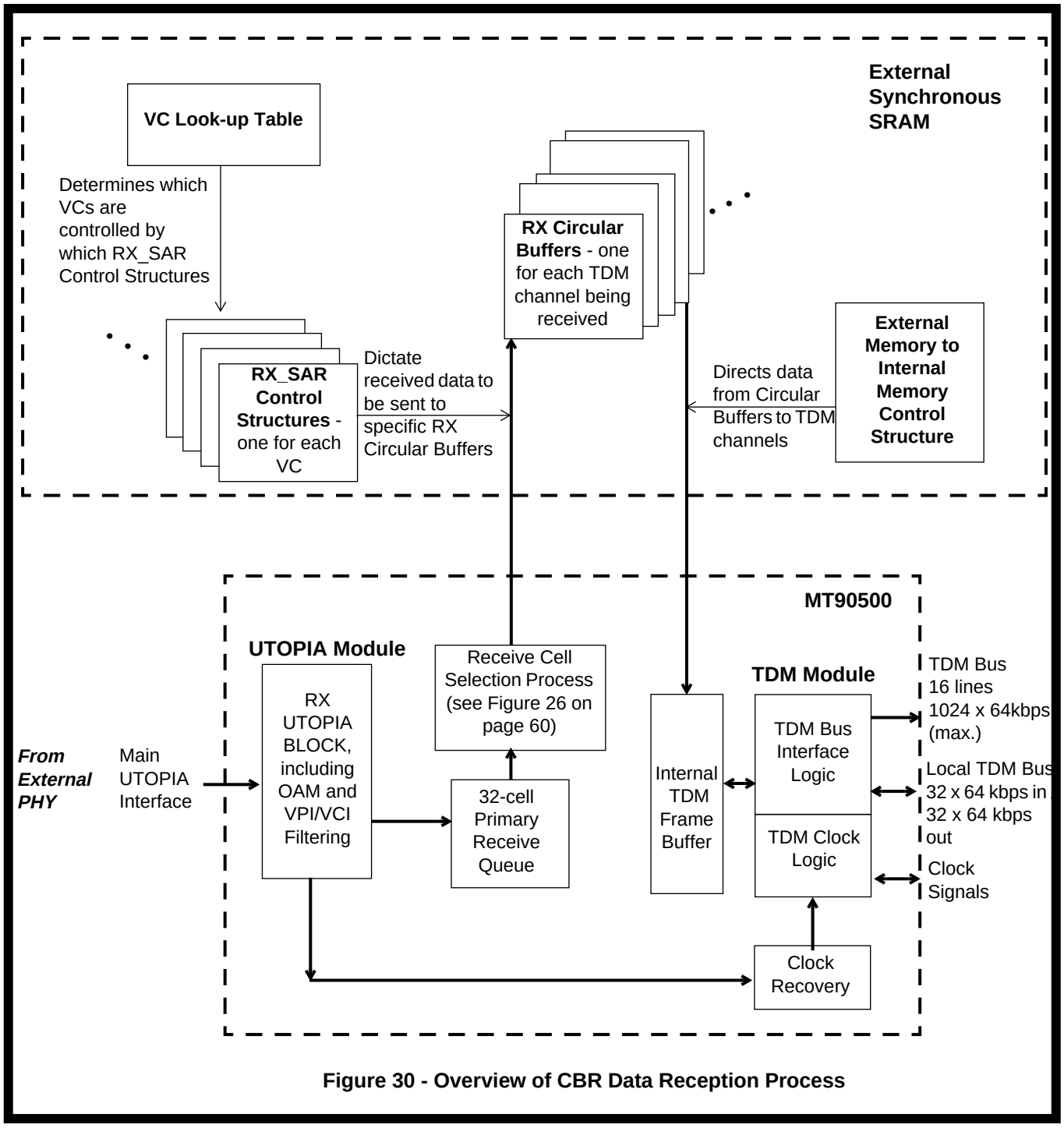


Figure 30 - Overview of CBR Data Reception Process

4.6 Clock Recovery from ATM Link

4.6.1 Adaptive Clock Recovery Sub-Module

Adaptive Clock Recovery is a flexible method for TDM clock recovery from an ATM link. There are several approaches to adaptive clock recovery, and the standards do not require a specific one, so adaptive clock recovery is termed “non-standardized.” The implementation given here is similar to the general outline in ITU-T I.363.1. In the MT90500, adaptive clock recovery uses a reference 8 kHz clock to generate the TDM clock signals. The TDM clocks are controlled by adjusting the reference 8 kHz clock frequency according to the arrival rate of ATM cells on a designated VC.

As seen in Figure 31, the reception rate of timing reference cells or 8 kHz markers (EX_8KA) is used as the basis for the adaptive clock recovery scheme implemented by this sub-module. This block is responsible for generating (under software control) a reference clock signal (RXVCLK) based on the rate of reception of the timing reference cells or markers. The sub-module additionally implements a state machine (seen in Figure 32) which tracks the cell arrival rate, checks the cell sequence numbers for lost or misinserted cells or cells with bad SNP fields (to a maximum of one), and adjusts for discrepancies.

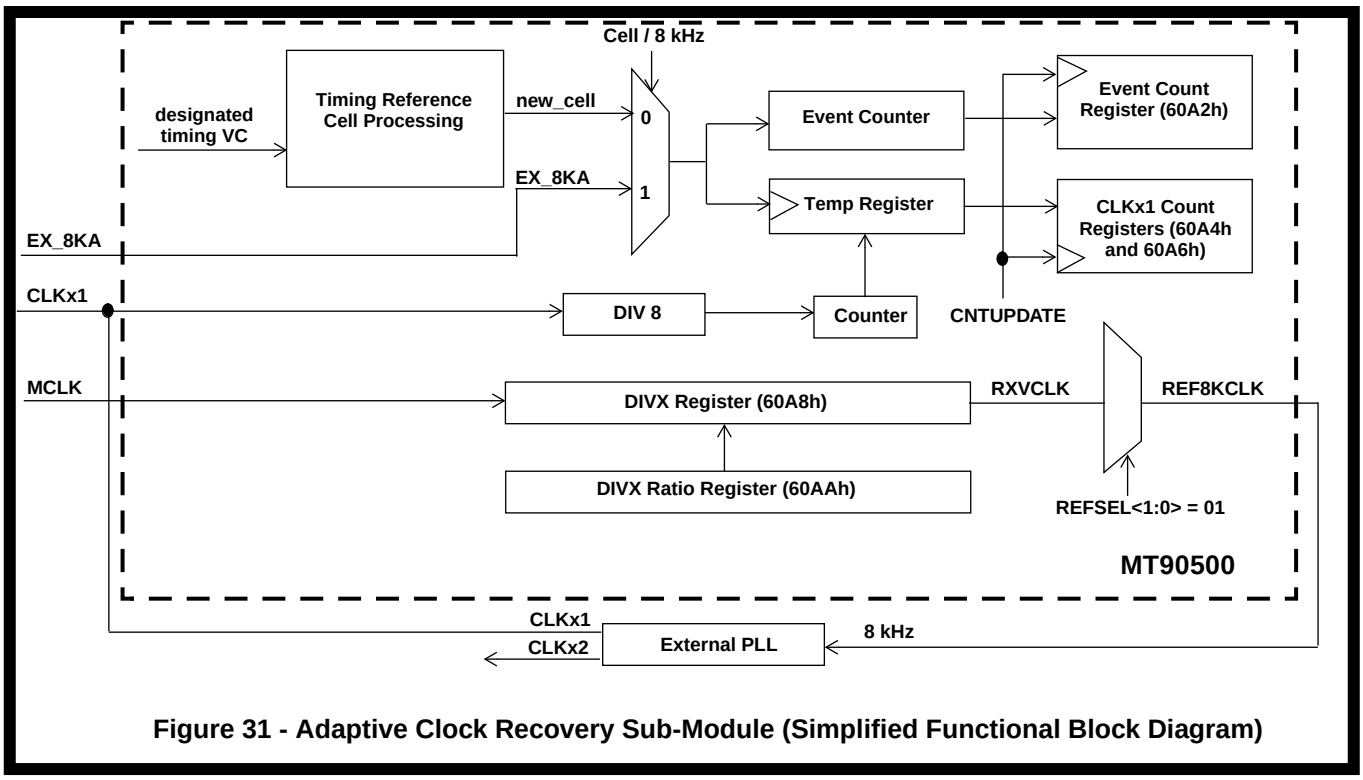
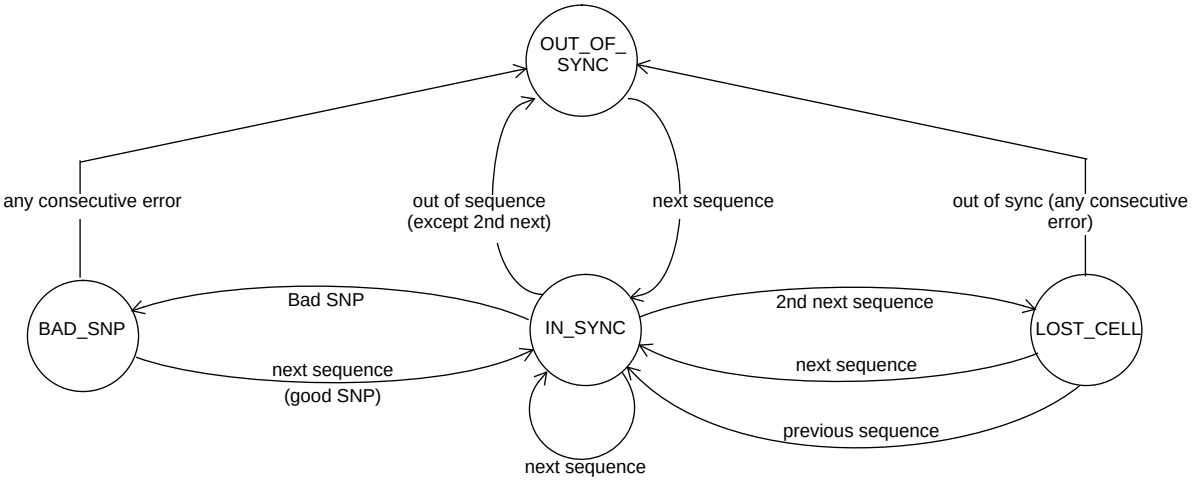


Figure 31 - Adaptive Clock Recovery Sub-Module (Simplified Functional Block Diagram)

The Adaptive Clock Recovery Block consists of:

- a Timing Reference Cell Processing unit which generates an event (“new_cell”) every time a timing reference cell is received. A timing reference cell is defined as an AAL1 cell whose VPI/VCI matches that specified in the VPI Timing Register (401Ah) and the VCI Timing Register (401Ch). OAM cells on the specified VPI/VCI are ignored, as they do not carry CBR data. The unit can compensate for a single lost or misinserted cell or bad sequence number protection (SNP). It will also flag an out-of-sync error when more than one cell is lost, misordered, or received with corrupted sequence number protection. SNP-checking is enabled by setting the Seq_CRC_Ena bit in the Timing Reference Processing Control Register at 60A0h. If no timing reference cell is received within a certain period (user-definable by setting bits<9:0> in the same register), it will generate a loss of timing reference cell error. The state machine for this unit is shown in Figure 32:



- When going to In_Sync or Bad SNP state, generate one timing reference pulse for each timing cell received. (“Bad SNP” is bad Sequence Number Protection, meaning a bad CRC, or a bad parity bit.)

- When going to Lost Cell state, generate two timing reference pulses.

- When coming back to In_Sync state from Lost Cell state, generate one pulse if “next sequence” received. Do not generate pulse if “previous sequence” received, indicating an inverse-ordered cell condition.

- When in Out_of_Sync state, do not generate timing pulses. If OUT_SYNC_IE bit is set at 6080h, and TIM_INTE is set at 0000h, an interrupt will be generated on entering Out_Of_Sync.

- If no timing reference cells or markers have been received within the time-out period set in the Timing Reference Processing Control Register (60A0h), a Loss of Timing Reference Cells event will be indicated (LOSS_TIMRF in 6082h), and an interrupt will be generated if LOSSCIE is set at 6080h (and TIM_INTE is set at 0000h).

Figure 32 - Timing Reference Cell Processing State Machine

- the Event Counter, which keeps a running count of the timing reference cells or 8 kHz markers received. The Cell/8 kHz bit in the Timing Reference Processing Control Register (address 60A0h) is used to select whether clock recovery is based on Timing Reference Cell arrival events, or 8 kHz marker events. The Event Count Register (60A2h) is updated every time the CNTUPDATE bit is set HIGH in the Clock Module General Control Register at 6080h.
- a counter which is incremented every eight cycles of CLKx1. The output of this counter is sent to the Temp Register, which is updated every time the Event Counter is incremented. Finally, the CLKx1 Count Registers (60A4h and 60A6h) are updated every time the CNTUPDATE bit is set HIGH in the Clock Module General Control Register at 6080h.

The RXVCLK Clock Generation Block is composed of:

- a programmable divider (DIVX Register at address 60A8h) which divides the master IC clock (MCLK) in order to obtain RXVCLK.
- a division factor register (DIVX Ratio Register at address 60AAh) which controls the ratio of divide-by-X to divide-by-(X+1).

Together, the Adaptive Clock Recovery Block and the RXVCLK Clock Generation Block allow the CPU to implement an adaptive algorithm which permits the locally generated TDM clock to track the remotely generated TDM clock.

The adaptive clock recovery method operates on a single receive VC which is defined by the VCI Timing Register and the VPI Timing Register. The clock recovery method is, briefly, as follows:

- Every (CLKx1 * 8) clock period, counter 1 (CLKx1 Counter) is incremented.
- Every time an 8 kHz marker or a cell with the Timing Recovery ID is received, counter 2 (Event Counter) is incremented. As well, the CLKx1 Counter value is latched to the Temp Register.
- Periodically, the processor writes the CNTUPDATE bit in Clock Module General Control Register (6080h) and reads both counters to determine if the local clock needs to be sped up or slowed down with respect to the remote clock.
- The local clock (RXVCLK) frequency is then adjusted by controlling the contents of the DIVX (60A8h) and DIVX Ratio (60AAh) Registers.

Please refer to the MT90500 Programmers' Manual for an example of an Adaptive Clock Recovery algorithm.

4.7 Microprocessor Interface

4.7.1 General

This interface allows an external control device (microprocessor) to configure and confirm the status of the MT90500 via access to internal control and status registers and access to the external device memories. It supports a variety of software maskable interrupt services.

The CPU interface allows external microprocessors to program the MT90500 and its external memory. The interface supports word (16-bit) data accesses only. The AEM pin determines if the access is to internal registers (‘0’), or to external memory (‘1’).

The CPU module features internal registers that are used to control and monitor the operation of the MT90500. See Main Control Register (0000h) and Main Status Register (0002h) in Section 5.2.

Detailed timing diagrams for the microprocessor interface are shown in Section 6.2.3, “CPU Interface - Accessing Registers and External Memory”.

4.7.2 A Programming Example - How to Set Up a VC

The basic sequence for initializing a connection at the MT90500 can be summarized in 5 functional steps.

In outlining the basic steps, we consider the need to allocate an ATM Virtual Circuit to one or more 64 kbps channels present at the ST-BUS interface (ST[15:0]). In this particular scenario, we focus on a channel to be received from the ST-BUS interface and sent out at the ATM interface (i.e. the transmit process). A similar procedure (albeit in the reverse order) will have to be repeated for the case whereby an ATM VC is received and transferred to the associated 64 kbps channel at the ST-BUS interface (i.e. the receive process).

1 - The CPU identifies which 64 kbps time slot(s) or N x 64 kbps grouped channel(s) must be selected on the ST-BUS backplane. The identification of the selected channels is done via a command from the driver managing the device.

2 - The CPU identifies which of the Transmit Circular Buffers are available to receive the 64 kbps time slots from the ST-BUS interface. The number of circular buffers available will depend on the number of time slots and the data rate selected at the ST-BUS backplane interface (256 time slots @ 2.048 Mbps, 512 time slots @ 4.096 Mbps or 1024 time slots @ 8.192 Mbps).

3 - Once the selection of the circular buffers is made, the CPU maps the time slots to be serviced and therefore to be transferred to the external circular buffers. This is performed via programmable pointers in the Transmit Circular Buffer Control Structure, located in external memory.

4 - The CPU starts filling the Transmit Control Structure(s). This information is programmed in external memory and identifies (in summary) the ATM cell header bytes, the circular buffer address(es) from which the device will take the time slots and assemble cells, and whether or not this is a partially-filled cell.

5 - Once the ATM cell structure for a particular VC is complete, the CPU can program the scheduler, which basically tells the MT90500 how many and which tasks must be executed every 125 µs.

If multiple ATM Virtual Circuits have to be opened simultaneously, the CPU can execute items 1 to 4 taking into consideration all the TDM channels being treated. However, item 5 can be optimized to provide some fairness in the general TX_SAR engine so that the device can perform up to 1024 specific ATM VC cell assembly functions using minimal memory and processing time requirements. The details of that operation, as well as specific VC setup examples, are provided in the MT90500 Programmers’ Manual.

4.8 Test Interface

The MT90500 contains an IEEE 1149 standard Test Access Port (TAP), which provides Boundary-Scan test access to aid board-level testing. (IEEE 1149 is often referred to by its older designation: JTAG - Joint Test Action Group.)

4.8.1 Test Access Port

The test port is a standard IEEE 1149 interface, with the optional $\overline{\text{TRST}}$ pin. The Test Access Port consists of 5 pins:

TCLK: Boundary-scan Test Clock.

TDI: Test Data In; input pin clocked in on the rising edge of TCK. TDI should be pulled HIGH if boundary-scan is not in use.

TDO: Test Data Out; output pin updated on the falling edge of TCK. The output is in high-impedance except when data is actually being shifted out.

TMS: Test Mode Select; input control line clocked in on the rising edge of TCK. TMS should be pulled HIGH if boundary-scan is not in use.

$\overline{\text{TRST}}$: Test Reset; asynchronous, active-low, input which is used to reset the JTAG interface, and the TAP controller. The $\overline{\text{TRST}}$ pin has an internal pull-down, and should also be pulled LOW externally whenever boundary-scan is not in use, to ensure normal operation of the MT90500. Figure 33 below shows a typical board-level design, including how $\overline{\text{TRST}}$ can be pulled HIGH by the test connector in cases where the tester does not provide a $\overline{\text{TRST}}$ pin.

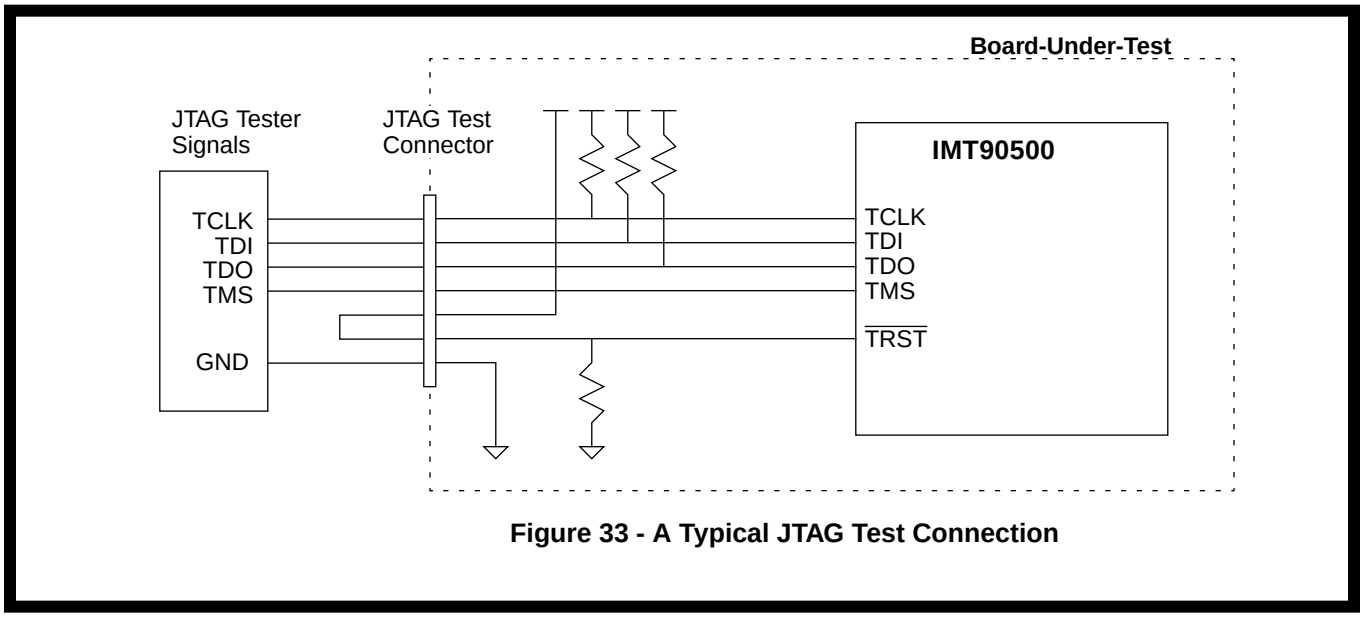


Figure 33 - A Typical JTAG Test Connection

4.8.2 JTAG ID

The JTAG device ID for the MT90500 is 0050014Bh:

Version<31:28>:	0000
Part Number<27:12>:	0000 0101 0000 0000 = 0500h
Manufacturer ID<11:1>:	0001 0100 101
LSB<0>:	1

4.8.3 Boundary Scan Instructions

The TAP Controller of the MT90500 supports the following instructions: IDCODE, SAMPLE, BYPASS, EXTEST, HIGHZ, CLAMP, and INTEST.

4.8.4 BSDL

A BSDL (Boundary Scan Description Language) file is available from Mitel Semiconductor to aid in the use of the IEEE 1149 test interface.

5. Register Map

5.1 Register Overview

5.1.1 General

This section describes the registers contained within the MT90500. The MT90500 is mapped over 128 Kbytes of address space, which is divided into two halves by the state of the AEM input pin. The division of the addressing allows the user to access either the internal registers associated with the different internal blocks, or to access the external SSRAM containing the circular buffers and associated control structures.

The first 64 Kbytes of address space are allocated for internal use, and are accessed by setting the AEM input pin low. As shown in Table 11 on page 72, the MT90500 does not implement all of the 64 Kbytes available inside the chip. The unused address space is reserved for future functionality.

The internal registers are used for control and status of:

- Microprocessor Interface
- TX_SAR
- RX_SAR
- UTOPIA module and interface
- TDM Interface and clock recovery
- TDM time slot control.

The second 64 Kbytes of address space are allocated as a window to external memory, accessed by setting the AEM input pin high. This window is used by the CPU to access up to 2048 Kbytes of external SRAM. The five latched address bits (EXTMADD[20:16] located at 0030h), provide access to 32 pages (each 64 Kbytes long) of external memory.

All microprocessor accesses are 16-bit (word) accesses; byte access is not supported. Note that addresses are however expressed as byte addresses. The least-significant-bit of the address bus is the A1 pin, sufficient to distinguish between 16-bit words.

All register addresses and reset values are listed in hexadecimal (Hex) format.

The register types are:

- Read / Write (R/W) - can be read or written via the microprocessor interface.
- Read Only Latched (R/O/L) - these bits are set by an activated status point within the chip; once set, they remain set even if the status point is deactivated. The microprocessor can read this point and clear it by writing a logic ‘1’ into it. The register is cleared if the status point is not active. Writing logic ‘0’ has no effect on this register.
- Read Only (R/O) - can be read via the microprocessor interface. A write to this register is ignored by the chip.
- Write Only (W/O) - certain bits associated with AAL5 operation which must be written high, but which read back low.

5.1.2 Interrupt Structure

The MT90500 uses a two-level interrupt structure, as shown in Figure 34. For each of five major modules (TX_SAR, RX_SAR, UTOPIA, TDM Interface and TDM Clock) there is a Status register containing one or more status bits, and a Control register containing corresponding mask bits (interrupt enable bits). There is also a Main Status Register, and a Main Control Register.

For an interrupt to be asserted at the $\overline{INT}$ pin, the following three conditions must be met: a status bit in one of the five module Status Registers must be asserted by an alarm event; the mask bit for that alarm event must be set in that modules Control Register; and the mask bit for that module must be set in the Main Control Register.

Similarly, an interrupt event at the $\overline{INT}$ pin can be traced back to its source by reading the Main Status Register to identify the module which is the source of the alarm, and then reading that module's Status Register to identify the particular alarm source. The interrupt can then be cleared by writing a '1' over the status bit.

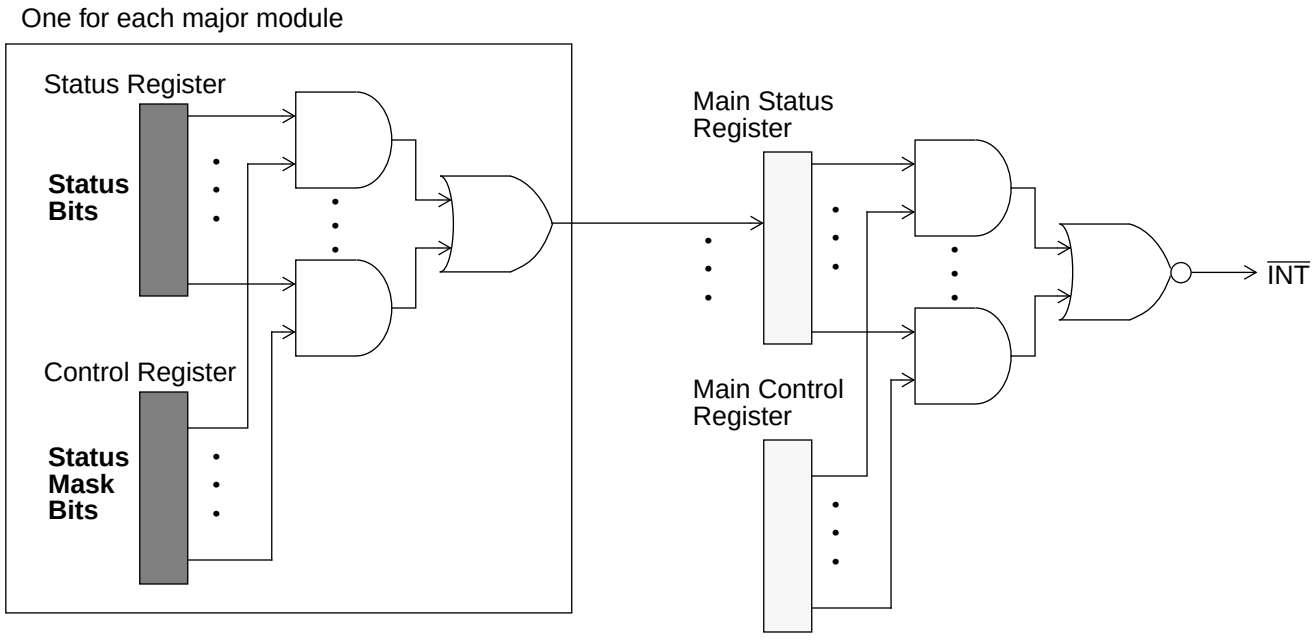


Figure 34. MT90500 Interrupt Structure

5.1.3 Register Summary

Table 11 - Register Summary

Address Hex	Label	Reset Value	Description
Microprocessor Interface Registers			
0000	MCR	0000	Main Control Register
0002	MSR	00X0	Main Status Register
0010	Reserved	0000	Reserved - DO NOT WRITE
0012	Reserved	0001	Reserved - DO NOT WRITE
0030	WTEMC	0000	Window to External Memory Register - CPU
0032	Reserved	0000	Reserved - DO NOT WRITE
0034	Reserved	0000	Reserved - DO NOT WRITE
0036	RDPAR	0000	Read Parity Register
0040	MEMCNF	0008	Memory Configuration Register
TX_SAR Registers			
2000	TXSC	0000	TX_SAR Control Register
2002	TXSS	0000	TX_SAR Status Register
2010	TESBAA	0000	TX_SAR Scheduler Base Register - Scheduler A
2012	TESFEA	0000	TX_SAR Frame End Register - Scheduler A
2014	TESERA	0000	TX_SAR End Ratio Register - Scheduler A
2020	TESBAB	0000	TX_SAR Scheduler Base Register - Scheduler B
2022	TESFEB	0000	TX_SAR Frame End Register - Scheduler B
2024	TESERB	0000	TX_SAR End Ratio Register - Scheduler B
2030	TESBAC	0000	TX_SAR Scheduler Base Register - Scheduler C
2032	TESFEC	0000	TX_SAR Frame End Register - Scheduler C
2034	TESERC	0000	TX_SAR End Ratio Register - Scheduler C
2040	TXCSBA	0000	TX_SAR Control Structure Base Address Register
2050	TXDFBA	0000	Transmit Data Cell FIFO Base Address Register
2052	TXDFWP	0000	Transmit Data Cell FIFO Write Pointer Register
2054	TXDFRP	0000	Transmit Data Cell FIFO Read Pointer Register
RX_SAR Registers			
3000	RXSCR	0000	RX_SAR Control Register
3002	RXSSR	0000	RX_SAR Status Register
3010	RXMEID	0000	RX_SAR Misc. Event ID Register
3012	RXMECT	0000	RX_SAR Misc. Event Counter Register
3020	RXUEID	0000	RX_SAR Underrun Event ID Register
3022	RXUECT	0000	RX_SAR Underrun Event Counter Register
3030	RXOEID	0000	RX_SAR Overrun Event ID Register
3032	RXOECT	0000	RX_SAR Overrun Event Counter Register
UTOPIA Registers			
4000	UCR	0000	UTOPIA Control Register
4002	USR	0000	UTOPIA Status Register
4010	VPVCC	0000	VPI / VCI Concatenation Register
4012	VPMT	0000	VPI Match Register
4014	VPMS	0000	VPI Mask Register
4016	VCMT	0000	VCI Match Register
4018	VCMS	0000	VCI Mask Register
401A	VPITIM	0000	VPI Timing Register

Table 11 - Register Summary

Address Hex	Label	Reset Value	Description
401C	VCITIM	0000	VCI Timing Register
401E	LUTBA	0000	Look-up Table Base Address Register
4020	RXDFBA	0000	Receive Data Cell FIFO Base Address Register
4022	RXDFWP	0000	Receive Data Cell FIFO Write Pointer Register
4024	RXDFRP	0000	Receive Data Cell FIFO Read Pointer Register
TDM Interface and Clock Interface Registers			
6000	TDMCNT	0000	TDM Interface Control Register
6002	TIS	XX00	TDM Interface Status Register
6004	CORSIG	0000	TDM I/O Register
6010	TDMTYP	0000	TDM Bus Type Register
6020	LBTYP	0000	Local Bus Type Register
6022	TDMLOC	0000	TDM Bus to Local Bus Transfer Register
6024	LOCTDM	0000	Local Bus to TDM Bus Transfer Register
6040	TXCBCS	0000	TX Circular Buffer Control Structure Base Register
6042	EMIM	0000	External to Internal Memory Control Structure Base Register
6044	TXCBBA	0000	TX Circular Buffer Base Address Register
6046	RXUNDA	0000	TDM Read Underrun Address Register
6048	RXUNDC	0000	TDM Read Underrun Count Register
6080	CMGCR	0000	Clock Module General Control Register
6082	CMGSR	0000	Clock Module General Status Register
6090	MCGCR	00C0	Master Clock Generation Control Register
6092	MCDF	2000	Master Clock / CLKx2 Division Factor
60A0	TRPCR	0001	Timing Reference Processing Control Register
60A2	EVCR	0000	Event Count Register
60A4	C1CRL	0000	CLKx1 Count - Low Register
60A6	C1CRH	0000	CLKx1 Count - High Register
60A8	DIVX	2000	DIVX Register
60AA	DIVXR	0FFF	DIVX Ratio Register
TDM Time Slot Control			
7000 + 2N	OEM	XXXX	Output Enable Registers (N=0,1,2,....,127)

5.2 Register Description

5.2.1 Microprocessor Interface Registers

Table 12 - Main Control Register

Address: 0000 (Hex) **Label: MCR** **Reset Value: 0000 (Hex)**			
Label	**Bit Position**	**Type**	**Description**
TDM_INTE	0	R/W	TDM Module Interrupt Enable. Enables interrupts from the TDM module when '1'. See TDM_SERV in Register 0002h.
TX_SAR_INTE	1	R/W	TX_SAR Module Interrupt Enable. Enables interrupts from the TX_SAR module when '1'. See TX_SAR_SERV in Register 0002h.
RX_SAR_INTE	2	R/W	RX_SAR Module Interrupt Enable. Enables interrupts from the RX_SAR module when '1'. See RX_SAR_SERV in Register 0002h.
MUX_INTE	3	R/W	UTOPIA MUX Sub-module Interrupt Enable. Enables interrupts from the UTOPIA module when '1'. See MUX_SERV in Register 0002h.
TIM_INTE	4	R/W	Timing Recovery Module Interrupt Enable. Enables interrupts from the Timing Recovery module when '1'. See TIM_SERV in Register 0002h.
Reserved	10:5	R/W	Reserved. Must be set to "100_000".
PAGE_MODE	11	R/W	For normal operation, set this bit to '1'.
PTXCLK_SEL	13:12	R/W	PTXCLK Select. Choose how PTXCLK is generated. "00"= PTXCLK pin is tristated (external oscillator drives the pin); "01"= MCLK/2; "10"= MCLK/4; "11"=STXCLK.
CLOCKMOD	14	R/W	Clock Mode. When '0', all external clocks (except MCLK) are replaced by MCLK/4. When '1', all clocks operate normally. This feature ensures that all flip-flops in the MT90500 are reset even if some secondary clocks are absent. To prevent internal clock glitches, this bit should be set before $\overline{\text{SRES}}$ is de-asserted.
$\overline{\text{SRES}}$	15	R/W	Software Reset. When '0', all modules except the CPU module are maintained in a reset state. Note that the MT90500 is synchronously reset, and that MCLK should be applied during reset. Reset should last at least 2 µsec when MCLK is 60 MHz (>75 clock cycles). **Note: $\overline{\text{SRES}}$ should be written to '1' before any other register is accessed.**

Table 13 - Main Status Register

Address: 0002 (Hex) **Label: MSR** **Reset Value: 00X0 (Hex)**			
Label	**Bit Position**	**Type**	**Description**
TDM_SERV	0	R/O	TDM Module Service Request. When '1', indicates the TDM module requires service (i.e. at least one TDM Interface event bit (in register 6002h) and matching enable bit (in register 6000h) are set). When this bit is '1' and the TDM_INTE interrupt enable bit is '1' in the MCR (Register 0000h), an external hardware interrupt is generated.
TX_SAR_SERV	1	R/O	TX_SAR Module Service Request. When '1', indicates the TX_SAR module requires service (i.e. at least one TX_SAR event bit (in register 2002h) and matching enable bit (in register 2000h) are set). When this bit is '1' and the TX_SAR_INTE interrupt enable bit is '1' in the MCR (Register 0000h), an external hardware interrupt is generated.
RX_SAR_SERV	2	R/O	RX_SAR Module Service Request. When '1', indicates the RX_SAR module requires service (i.e. at least one RX_SAR event bit (in register 3002h) and matching enable bit (in register 3000h) are set). When this bit is '1' and the RX_SAR_INTE interrupt enable bit is '1' in the MCR (Register 0000h), an external hardware interrupt is generated.
MUX_SERV	3	R/O	UTOPIA MUX Sub-module Service Request. When '1', indicates the UTOPIA MUX sub-module requires service (i.e. at least one UTOPIA event bit (in register 4002h) and matching enable bit (in register 4000h) are set). When this bit is '1' and the MUX_INTE interrupt enable bit is '1' in the MCR (Register 0000h), an external hardware interrupt is generated.

Table 13 - Main Status Register

Address: 0002 (Hex)
Label: MSR
Reset Value: 00X0 (Hex)

Label	Bit Position	Type	Description
TIM_SERV	4	R/O	Timing Module Service Request. When '1', indicates the Timing Recovery module requires service (i.e. at least one Clock Recovery event bit (in register 6082h) and matching enable bit (in register 6080h) are set. When this bit is '1' and the TIM_INTE interrupt enable bit is '1' in the MCR (Register 0000h), an external hardware interrupt is generated.
Reserved	6:5	R/0	Reserved. Undefined at reset.
SERVICE	7	R/O	'1' when any of bits<4:0> is set. Undefined at reset.
Reserved	15:8	R/O	Always read "0000_0000"

Table 14 - Window to External Memory Register - CPU

Address: 0030 (Hex)
Label: WTEMC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
EXTMADD16	0	R/W	This bit represents address line A[16] for external memory access. This bit maps to MEM_ADD[14].
EXTMADD17	1	R/W	This bit represents address line A[17] for external memory access. This bit maps to MEM_ADD[15] or bank_selection (32K addressing mode).
EXTMADD18	2	R/W	This bit represents address line A[18] for external memory access. This bit maps to MEM_ADD[16] or bank_selection (64K addressing mode).
EXTMADD19	3	R/W	This bit represents address line A[19] for external memory access. This bit maps to MEM_ADD[17] or bank_selection (128K addressing mode).
EXTMADD20	4	R/W	This bit represents address line A[20] for external memory access. This bit maps to bank_selection (256K addressing mode).
Reserved	15:5	R/W	Reserved, must always be "0000_0000_000".
This register is automatically used while a CPU access is performed.			

Table 15 - Read Parity Register

Address: 0036 (Hex)
Label: RDPAR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CPUPAR32	0	R/O	Bit 32 corresponds to the parity bit of the MS byte of the last odd word read from the external memory by the CPU.
CPUPAR33	1	R/O	Bit 33 corresponds to the parity bit of the LS byte of the last odd word read from the external memory by the CPU.
CPUPAR34	2	R/O	Bit 34 corresponds to the parity bit of the MS byte of the last even word read from the external memory by the CPU.
CPUPAR35	3	R/O	Bit 35 corresponds to the parity bit of the LS byte of the last even word read from the external memory by the CPU.
Reserved	7:4	R/O	Reserved.
Reserved	15:6	R/O	Reserved. Always read "0000_0000".

Table 16 - Memory Configuration Register

Address: 0040 (Hex)
Label: MEMCNF
Reset Value: 0008 (Hex)

Label	Bit Position	Type	Description
ADDMODE	1:0	R/W	Addressing Mode. Indicates the number of address lines connected to the external memory and therefore the size of the memory chip(s). “00”=32K (MEM_ADD[14:0]); “01”=64K (MEM_ADD[15:0]); “10”=128K (MEM_ADD[16:0]); “11”=256K (MEM_ADD[17:0]).
CPBANK	2	R/W	External Memory Chips per Bank. Indicates the number of external memory devices used in one memory bank. ‘0’=1 x 32 (36)-bit chip; ‘1’=2 x 16 (18)-bit chips.
READLEN	5:3	R/W	Read Length. Indicates the number of clock cycles between an address and its read data. “001”=1 clock cycle (used with “Synchronous Burst RAMs”); “010”=2 clock cycles (used with “Pipeline Synchronous Burst RAMs”); “100”=3 clock cycles; all other values are reserved. Writing a reserved value in this register may have adverse effects on the MT90500 and the external memories.
RWTA	6	R/W	Read/Write Turn Around Cycles. ‘0’=Disabled; ‘1’=Enabled.
RRTA	7	R/W	Read Bank1 / Read Bank2 Turn Around Cycles. ‘0’=Disabled; ‘1’=Enabled.
Reserved	15:8	R/W	Reserved. These bits must always be “0000_0000” during operation.

For further details on memory configuration, see Section 4.2, “External Memory Controller,” on page 36.

5.2.2 TX_SAR Registers

Table 17 - TX_SAR Control Register

Address: 2000 (Hex)
Label: TXSC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SAENA	0	R/W	Scheduler A Enable. '0' = Disabled; '1' = Enabled. Before enabling this scheduler, all its configuration registers must be written and valid. These registers must not be changed while SAENA is HIGH. If an event scheduler is re-configured (i.e. changes made to 2010h, 2012h, or 2014h), all of its events and dependent structures should be re-initialized before starting the scheduler again.
SBENA	1	R/W	Scheduler B Enable. '0' = Disabled; '1' = Enabled. Before enabling this scheduler, all its configuration registers must be written and valid. These registers must not be changed while SBENA is HIGH. If an event scheduler is re-configured (i.e. changes made to 2020h, 2022h, or 2024h), all of its events and dependent structures should be re-initialized before starting the scheduler again.
SCENA	2	R/W	Scheduler C Enable. '0' = Disabled; '1' = Enabled. Before enabling this scheduler, all its configuration registers must be written and valid. These registers must not be changed while SCENA is HIGH. If an event scheduler is re-configured (i.e. changes made to 2030h, 2032h, or 2034h), all of its events and dependent structures should be re-initialized before starting the scheduler again.
TXFFENA	3	R/W	Transmit FIFO Enable. When this bit is LOW, the Transmit Data Cell FIFO Read Pointer (TXFFRP in TXDFRP at 2054h) is reset to 00h. When this bit is HIGH, the FIFO can operate normally.
AUTODATA	4	R/W	When this bit is '1', non-CBR data cells (the next cells located in the Transmit Data Cell FIFO) will be transmitted while the TX_SAR is idle. When this bit is '0', data cell transmission is controlled by the schedulers.
TXFFORIE	5	R/W	Transmit Data Cell FIFO Overrun Error Interrupt Enable. '0' = Disabled; '1' = Enabled. When enabled, a '1' on TXFFOR in Register 2002h will force a '1' on TX_SAR_SERV in Register 0002h.
SCHEDULE_IE	6	R/W	Scheduler Error Interrupt Enable. '0' = Disabled; '1' = Enabled. When enabled, a '1' on SCHEDULE in Register 2002h will force a '1' on TX_SAR_SERV in Register 0002h.
TXFFRP+	7	R/W	Increment Transmit Data Cell FIFO Read Pointer. When '1' is written to this bit, the Transmit Data Cell FIFO Read Pointer (TXFFRP) is incremented.
TESTS	8	R/W	Test Status. When HIGH, this bit forces all the status events in TX_SAR Status Register at 2002h to occur. Used for test purposes only.
Reserved	15:9	R/O	Reserved. Always read as "0000_000".

Table 18 - TX_SAR Status Register

Address: 2002 (Hex)
Label: TXSS
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	4:0	R/O	Reserved. Always read as "0_0000".
TXFFOR	5	R/O/L	Transmit Data FIFO Overrun. When set, this bit indicates that the CPU changed the value of the Transmit Data Cell FIFO Write Pointer (2052h) to the value of the Transmit Data Cell FIFO Read Pointer (2054h). When this event occurs, the MT90500 assumes that the CPU is trying to write one more non-CBR cell than the FIFO can contain. Writing a '1' over this bit clears it.

Table 18 - TX_SAR Status Register

Address: 2002 (Hex)
Label: TXSS
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SCHEDULE	6	R/O/L	Scheduler Error. The TX_SAR has too heavy a work load (e.g. too many events per scheduler frame; uneven distribution of events throughout the scheduler). To recover, the schedulers must be stopped and re-balanced. The TX Control Structures must also be re-initialized. Writing a '1' over this bit clears it. **Fatal error.**
Reserved	14:7	R/O	Reserved. Always read as "000_0000_0".
TXSERV	15	R/W	TX Service. This bit is set if bit<5> or bit<6> is set.

Table 19 - TX_SAR Scheduler Base Register

Address: Scheduler A: 2010 (Hex); Scheduler B: 2020 (Hex); Scheduler C: 2030 (Hex)
Label: TESBAA; TESBAB; TESBAC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SBASE	11:0	R/W	Scheduler Base Address. This register contains bits<20:9> of the base address of an event scheduler. Bits<8:0> are always 000h. This register must not be changed when the scheduler is enabled.
ENTRY	15:12	R/W	Entries per Frame. This register contains the number of entries in one frame on the scheduler. "0000" = 8 entries; "0001" = 16 entries; "0010" = 32 entries; all other values are reserved. This register must not be changed when the scheduler is enabled.

Note: All scheduler entries must be read from external SSRAM to check if they are active or inactive. Better memory-bandwidth efficiency is achieved with fewer entries-per-frame and events distributed throughout the frames of the scheduler, as opposed to having bursts of events and many inactive entries.

Table 20 - TX_SAR Frame End Register

Address: Scheduler A: 2012 (Hex); Scheduler B: 2022 (Hex); Scheduler C: 2032 (Hex)
Label: TESFEA; TESFEB; TESFEC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SHTEND	7:0	R/W	Short End Frame. This register indicates the number of the last frame when the scheduler is executing a short turn. This register must not be changed when the scheduler is enabled.
LNGEND	15:8	R/W	Long End Frame. This register indicates the number of the last frame when the scheduler is executing a long turn. This register must not be changed when the scheduler is enabled.

Table 21 - TX_SAR End Ratio Register

Address: Scheduler A: 2014 (Hex); Scheduler B: 2024 (Hex); Scheduler C: 2034 (Hex)
Label: TESERA; TESERB; TESERC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
RATIO	2:0	R/W	Long/Short Ratio. This register indicates how many long turns a scheduler must execute for one short turn. In other words, the value in this register is the non-P : P-cell ratio. For pointerless cells, the value must be "000". For structured cells, the value can be "001" (1:1), "011" (3:1), or "111" (7:1). This register must not be changed when the scheduler is enabled.

Table 21 - TX_SAR End Ratio Register

Address: Scheduler A: 2014 (Hex); Scheduler B: 2024 (Hex); Scheduler C: 2034 (Hex)
Label: TESERA; TESERB; TESERC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
SINGLE	3	R/W	Single Frame Assembly. When '1', this bit indicates that cells must be assembled one frame at a time, which allows an even cell flow. When it is '0', it indicates that cells are formed 4 frames at a time, which allows better external memory efficiency. This register must not be changed when the scheduler is enabled. For full 1024 VC (or 1024 TDM time slot) operation, this bit must be '0'.
Reserved	5:4	R/W	Reserved. These bits must always be written as "00".
AAL5_INIT	7:6	W/O	Initialization bits for AAL5 operation. These two bits must be written, at initialization, in **all** three schedulers for AAL5 operation in **any** scheduler, regardless of how many schedulers are active. The INIT pattern is different in each of the three schedulers: 2014h, Scheduler A(7:6) : '01' 2024h, Scheduler B(7:6) : '10' 2034h, Scheduler C(7:6) : '11'
Reserved	15:8	R/O	Reserved. These bits must always be "0000_0000".

Table 22 - TX_SAR Control Structure Base Address Register

Address: 2040 (Hex)
Label: TXCSBA
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXBASE	4:0	R/W	TX Control Structure Base Address. When accessing a Transmit Control Structure, TXBASE represents address bits<20:16>; the address in the scheduler, bits<15:4>. This register must not be changed when any scheduler is enabled.
Reserved	15:5	R/O	Reserved. Always read as "0000_0000_000".

Table 23 - Transmit Data Cell FIFO Base Address Register

Address: 2050 (Hex)
Label: TXDFBA
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXFFBASE	11:0	R/W	Transmit Data Cell FIFO Base Address. Represents address bits<20:9> that point to the first structure in the Transmit Data Cell FIFO. The lower bits of this pointer are "0_0000_0000". Each non-CBR cell occupies a 64-byte buffer. The Transmit Data Cell FIFO must not overlap an 8 Kbyte boundary. When this register is changed, TXFFENA (in the TX_SAR Control Register at 2000h) must not be asserted.
TXFFSIZ	13:12	R/W	Transmit Data Cell FIFO Size. This field indicates the number of non-CBR data cells in the Transmit Data Cell FIFO. "00"=16 cells; "01"=32 cells; "10"=64 cells; "11"=128 cells. When this register is changed, TXFFENA (in the TX_SAR Control Register at 2000h) must not be asserted.
Reserved	15:14	R/W	Reserved. Always read as "00".

Table 24 - Transmit Data Cell FIFO Write Pointer Register

Address: 2052 (Hex)
Label: TXDFWP
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXFFWP	7:0	R/W	Transmit Data Cell FIFO Write Pointer. Indicates cell structure number in which the CPU is currently writing (the cell is not yet valid) within the Transmit Data Cell FIFO.
Reserved	15:8	R/O	Reserved. Always read as 00h.

Table 25 - Transmit Data Cell FIFO Read Pointer Register

Address: 2054 (Hex)
Label: TXDFRP
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXFFRP	6:0	R/O	Transmit Data Cell FIFO Read Pointer. Indicates the cell structure number in which the TX_SAR is currently transmitting (the cell is still valid).
Reserved	15:7	R/O	Reserved. Always read as “0000_0000_0”.

5.2.3 RX_SAR Registers

Table 26 - RX_SAR Control Register

Address: 3000 (Hex)
Label: RXSCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
APEMS	0	R/W	AAL1-byte Parity Error Misc. Select. When this bit is set, a parity error in the AAL1-byte increments the RX_SAR Misc. Event Counter Register (3012h) and affects the RX_SAR Misc. Event ID Register (3010h).
ACEMS	1	R/W	AAL1-byte CRC Error Misc. Select. When this bit is set, a CRC error in the AAL1-byte increments the RX_SAR Misc. Event Counter Register (3012h) and affects the RX_SAR Misc. Event ID Register (3010h).
SNEMS	2	R/W	AAL1 Sequence Number Error Misc. Select. When this bit is set, a sequence number error in the AAL1-byte increments the RX_SAR Misc. Event Counter Register (3012h) and affects the RX_SAR Misc. Event ID Register (3010h).
PPEMS	3	R/W	Pointer-byte Parity Error Misc. Select. When this bit is set, a parity error in the pointer-byte (for P-Type cells only) increments the RX_SAR Misc. Event Counter Register (3012h) and affects the RX_SAR Misc. Event ID Register (3010h).
POREMS	4	R/W	Pointer-byte Out of Range Error Misc. Select. When this bit is set, an out of range pointer-byte (for P-Type cells only) increments the RX_SAR Misc. Event Counter Register (3012h) and affects the RX_SAR Misc. Event ID Register (3010h).
APEIE	5	R/W	AAL1-byte Parity Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on APE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h.
ACEIE	6	R/W	AAL1-byte CRC Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on ACE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
SNEIE	7	R/W	AAL1-byte Sequence Number Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on SNE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
PPEIE	8	R/W	Pointer-byte Parity Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on PPE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
POREIE	9	R/W	Pointer-byte Out of Range Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on PORE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
WUREIE	10	R/W	Write Underrun Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on WURE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
WOREIE	11	R/W	Write Overrun Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on WORE in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
MCRIE	12	R/W	Misc. Counter Rollover Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on MCR in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
WURCRIE	13	R/W	Write UnderRun Counter Rollover Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on WURCR in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
WORCRIE	14	R/W	Write Overrun Counter Rollover Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on WORCR in Register 3002h will force a ‘1’ on RX_SAR_SERV in Register 0002h
TESTS	15	R/W	Test Status. When HIGH, this bit forces all the status events in the RX_SAR Status Register at 3002h to occur. Also increments the RX_SAR Misc. Event Counter Register (3012h), the RX_SAR Underrun Event Counter (3022h), and the RX_SAR Overrun Event Counter (3032h) and affects the contents of the RX_SAR Misc. Event ID Register (3010h), the RX_SAR Underrun Event ID Register (3020h), and the RX_SAR Overrun Event ID Register (3030h). Used for test purposes only.

Table 27 - RX_SAR Status Register

Address: 3002 (Hex)
Label: RXSSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	4:0	R/O	Reserved. Always read as “0_0000”.
APE	5	R/O/L	AAL1-byte Parity Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
ACE	6	R/O/L	AAL1-byte CRC Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
SNE	7	R/O/L	AAL1-byte Sequence Number Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
PPE	8	R/O/L	Pointer-byte Parity Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
PORE	9	R/O/L	Pointer-byte Out of Range Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
WURE	10	R/O/L	Write Underrun Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
WORE	11	R/O/L	Write Overrun Error. ‘0’ = Event has not occurred. ‘1’ = Event has occurred. Writing a ‘1’ over this bit clears it.
MCR	12	R/O/L	Misc. Counter Rollover. If set, the RX_SAR Misc. Event Counter Register at 3012h has rolled over. Writing a ‘1’ over this bit clears it.
WURCR	13	R/O/L	Write Underrun Counter Rollover. If set, the RX_SAR Underrun Event Counter Register at 3022h has rolled over. Writing a ‘1’ over this bit clears it.
WORCR	14	R/O/L	Write Overrun Counter Rollover. If set, the RX_SAR Overrun Event Counter Register at 3032h has rolled over. Writing a ‘1’ over this bit clears it.
RXSERV	15	R/O/L	RX Service. This bit is set if any of bits<14:5> in this register is set. Writing a ‘1’ over this bit clears it.

Table 28 - RX_SAR Misc. Event ID Register

Address: 3010 (Hex)
Label: RXMEID
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
MISCID	15:0	R/W	MISC. Event ID number. This 16-bit register holds bits<19:4> of the address of the RX Control Structure that caused the last miscellaneous error. This register is only affected by the miscellaneous errors that are selected via the 5 least significant bits of the RX_SAR Control Register (3000h). This register will also be updated if the TESTS bit is set in the RX_SAR Control Register.

Table 29 - RX_SAR Misc. Event Counter Register

Address: 3012 (Hex)
Label: RXMECT
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
MISCC	15:0	R/W	MISC. Event Count. This 16-bit register’s value is incremented each time a miscellaneous error occurs. A miscellaneous error is considered to have occurred if any of bits<9:5> in the RX_SAR Status Register at 3002h is set and the corresponding miscellaneous select bit in bits<4:0> of the RX_SAR Control Register (3000h) is also set. This register is also incremented if TESTS is set in the RX_SAR Control Register.

Table 30 - RX_SAR Underrun Event ID Register

Address: 3020 (Hex)
Label: RXUEID
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
WURID	15:0	R/W	RX_SAR Write Underrun ID Number. This 16-bit register holds bits<19:4> of the address of the RX Control Structure that caused the last write underrun error. This register will also be updated if the TESTS bit is set in the RX_SAR Control Register at 3000h.

Table 31 - RX_SAR Underrun Event Counter Register

Address: 3022 (Hex)
Label: RXUECT
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
WURC	15:0	R/W	RX_SAR Write Underrun Count. This 16-bit register's value is incremented each time a write underrun occurs or if the TESTS bit is set in the RX_SAR Control Register at 3000h.

Table 32 - RX_SAR Overrun Event ID Register

Address: 3030 (Hex)
Label: RXOEID
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
WORID	15:0	R/W	RX_SAR Write Overrun ID Number. This 16-bit register holds bits<19:4> of the address of the RX Control Structure that caused the last write overrun error. This register will also be updated if the TESTS bit is set in the RX_SAR Control Register at 3000h.

Table 33 - RX_SAR Overrun Event Counter Register

Address: 3032 (Hex)
Label: RXOECT
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
WORC	15:0	R/W	RX_SAR Write Overrun Count. This 16-bit register is incremented each time a write overrun occurs or if the TESTS bit is set in the RX_SAR Control Register at 3000h.

5.2.4 UTOPIA Registers

Table 34 - UTOPIA Control Register

Address: 4000 (Hex)
Label: UCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
RXENA	0	R/W	RX Cell Enable. When ‘0’, all received cells are ignored. When ‘1’, received cells are processed normally.
STXENA	1	R/W	Secondary TX Cell Enable. When this bit is ‘0’, no cells may be received from the secondary TX interface. When ‘1’, the UTOPIA module receives cells from the secondary SAR normally.
RRP	2	R/W	Round-Robin Priority. When ‘0’, CBR traffic from the MT90500 has priority over traffic from the secondary SAR interface. When ‘1’, both traffic types have the same priority.
RXFFENA	3	R/W	Receive FIFO Enable. When this bit is LOW, the Receive Data Cell FIFO Write Pointer (RXFFWP at 4022h) is reset to 00h. When this bit is HIGH, the FIFO can operate normally.
RXFFWP+	4	R/W	Increment Receive Data Cell FIFO Write Pointer. When ‘1’ is written on this bit, the Receive Data Cell FIFO Write Pointer (RXFFWP at 4022h) is incremented.
OAMSEL	5	R/W	OAM Routing Select. ‘0’ = discard; ‘1’= treat as non-CBR data cell.
UKSEL	6	R/W	Unknown Routing Select. ‘0’ = discard cells with undefined entry types (i.e. T bits = “00” in look-up table); ‘1’= treat cells with undefined entry types (i.e. T bits = “00” in look-up table) as non-CBR data cells.
RXBASE	9:7	R/W	RX Control Structure Base Address. These three bits represent the three most significant address bits<20:18> of the pointer to the Receive Control Structures.
RXFFORIE	10	R/W	Receive Data Cell FIFO Overrun Error Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on RXFFOR in Register 4002h will force a ‘1’ on MUX_SERV in Register 0002h.
RXORIE	11	R/W	RX UTOPIA Module Internal FIFO Overrun Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on RXOR in Register 4002h will force a ‘1’ on MUX_SERV in Register 0002h.
RXFFRCIE	12	R/W	Receive Data FIFO Receive Cell Interrupt Enable. ‘0’ = Disabled; ‘1’ = Enabled. When enabled, a ‘1’ on RXFFRC in Register 4002h will force a ‘1’ on MUX_SERV in Register 0002h.
Reserved	14:13	R/W	Reserved. Should be written as “00”.
TESTS	15	R/W	TEST Status. When HIGH, this bit forces the three status events (bits<12:10>) in the UTOPIA Status Register at 4002h to occur. Used for test purposes only.

Table 35 - UTOPIA Status Register

Address: 4002 (Hex)
Label: USR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	9:0	R/O	Reserved. Always read as “00_0000_0000”.
RXFFOR	10	R/O/L	Receive Data Cell FIFO Overrun Error. When this bit is ‘1’, the RXFFWP (register 4022h) = RXFFRP (register 4024h) and one or more non-CBR data cells were discarded because the Receive Data Cell FIFO was full. Writing a ‘1’ over this bit clears it.
RXOR	11	R/O/L	Receive UTOPIA Module Internal FIFO Overrun. At least one CBR cell was lost because the RX_SAR did not process the cells fast enough. Writing a ‘1’ over this bit clears it.
RXFFRC	12	R/O/L	Data FIFO Receive Cell. Each time a non-CBR data cell is received, this bit is set. Writing a ‘1’ over this bit clears it.
Reserved	14:13	R/O	Reserved. Always read as “00”.
UTOSERV	15	R/O	UTOPIA Service. When any of the status bits in this register are HIGH, this bit is HIGH.

Table 36 - VPI / VCI Concatenation Register

Address: 4010 (Hex)
Label: VPVCC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
N	4:0	R/W	The N least significant bits of the VCI to be used as an address in the VC look-up table.
M	7:5	R/W	The M least significant bits of the VPI to be used as an address in the VC look-up table.
Reserved	8	R/W	Reserved. Must be written as ‘0’.
Reserved	15:9	R/O	Reserved. Always read as “0000_000”.

The VC search mechanism uses a table that can have up to 32K double-word (32-bit) entries. The table can therefore be 128 Kbytes long. This requires a 17-bit offset pointer formed by adding two least significant zeroes to a base 15-bit pointer. The base 15-bit pointer is formed by concatenating together the N least significant bits of the VCI with the M least significant bits of the VPI. The sum of M+N must be at least 8 and a maximum of 15. If M+N < 15, the most significant bits are zeroed.
Example: assume N=8, indicating that the 8 LSBs of the VCI will be used to form the least significant part of the pointer. Assume M=4, indicating that the 4 LSBs of the VPI will be used to form the most significant portion of the pointer. Since M+N = 12 < 15, bits<14:12> of the base pointer will be zeroed. Assume the receive VPI value is 23h and the receive VCI value is 5678h. The resulting base 15-bit pointer will be “0378.” When two least significant ‘0’ bits are added to form a 17-bit pointer, the result is 00DE0h. This value is added to the Look-up Table Base Address Register (401Eh) contents to form a 21-bit address than can be located anywhere in memory.

Table 37 - VPI Match Register

Address: 4012 (Hex)
Label: VPMT
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VPIMATCH	7:0	R/W	VPI Match value. VPI of received cells are compared to the value in this register to see if the cells should be passed to the internal FIFO, or discarded.
Reserved	15:8	R/O	Reserved. Always read as 00h.

Note: Set the VPI Match and Mask filter as narrowly as practical for the application. See Receive Cell Selection Process on page 58.

Table 38 - VPI Mask Register

Address: 4014 (Hex)
Label: VPMS
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VPIMASK	7:0	R/W	VPI Mask value. Each bit, when set, enables the comparison of the cell VPI and the VPIMATCH field. If a bit in this register is not set, the corresponding bit in the received cell VPI is considered valid, regardless of the setting in the VPIMATCH field.
Reserved	15:8	R/O	Reserved. Always read as 00h.

Table 39 - VCI Match Register

Address: 4016 (Hex)
Label: VCMT
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
VCIMATCH	15:0	R/W	VCI Match value. VCI of received cells are compared to the value in this register to see if the cells are valid.

Note: Set the VCI Match and Mask filter as narrowly as practical for the application. See Receive Cell Selection Process on page 58.

Table 40 - VCI Mask Register

Address: 4018 (Hex) Label: VCMS Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
VCIMASK	15:0	R/W	VCI Mask value. Each bit, when set, enables the comparison of the cell VCI and the VCIMATCH field. If a bit in this register is not set, the corresponding bit in the received cell VCI is considered valid, regardless of the setting in the VCIMATCH field.

Table 41 - VPI Timing Register

Address: 401A (Hex) Label: VPITIM Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
TIMING VPI	7:0	R/W	VPI of the timing reference VC. If the VPI_VCI of the incoming cell matches that contained within this register and the VCI Timing Register at 401Ch, a clock pulse will be sent to the clock recovery module.
Reserved	15:8	R/O	Reserved. Always read as 00h.

Table 42 - VCI Timing Register

Address: 401C (Hex) Label: VCITIM Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
TIMING VCI	15:0	R/W	VCI of the timing reference VC. If the VPI_VCI of the incoming cell matches that contained within this register and the VPI Timing Register at 401Ah, a clock pulse will be sent to the clock recovery module.

Table 43 - Lookup Table Base Address Register

Address: 401E (Hex) Label: LUTBA Reset Value: 0000 (Hex)			
Label	**Bit Position**	**Type**	**Description**
LUTBASE	15:0	R/W	Look-Up Table Base Address. Represents bits<20:5> of the pointer to the look-up table (bits<4:0> are “0_0000”). It must point to a boundary larger than or equal to K * {2^(M+N+2)} bytes, where K = 0,1,2,... and M and N are those values obtained from VPI/VCI Concatenation Register at address 4010h. In addition, the look-up table requires an external memory allocation of 2^(M+N+2) bytes to accommodate the entire look-up table.

Table 44 - Receive Data Cell FIFO Base Address Register

Address: 4020 (Hex)
Label: RXDFBA
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
RXFFBASE	11:0	R/W	Receive Data Cell FIFO Base Address. Represents address bits <20:9> that point to the first structure in the Receive Data Cell FIFO. The lower address bits <8:0> of the pointer are “0_0000_0000”. Each cell occupies a 64-byte buffer. Bit<0> of this field must always be ‘0’. The Receive Data Cell FIFO must not overlap an 8 Kbyte boundary. When this register is changed, FFENA in the UTOPIA Control Register at 4000h must not be asserted.
RXFFSIZ	13:12	R/W	Receive Data Cell FIFO Size. This field contains the number of non-CBR data cells in the Receive Data Cell FIFO. “00”=16 cells; “01”=32 cells; “10”=64 cells; “11”=128 cells. When this register is changed, FFENA in the UTOPIA Control Register at 4000h must not be asserted.
Reserved	15:14	R/W	Reserved. Always read as “00”.

Table 45 - Receive Data Cell FIFO Write Pointer Register

Address: 4022 (Hex)
Label: RXDFWP
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
RXFFWP	7:0	R/O	Receive Data Cell FIFO Write Pointer. Indicates cell structure number in which the UTOPIA module is currently writing (the cell is not valid yet) within the Receive Data Cell FIFO.
Reserved	15:8	R/O	Reserved. Always read as 00h.

Table 46 - Receive Data Cell FIFO Read Pointer Register

Address: 4024 (Hex)
Label: RXDFRP
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
RXFFRP	7:0	R/W	Receive Data Cell FIFO Read Pointer. Indicates the cell structure number in which the CPU is currently reading (the cell is still valid).
Reserved	15:8	R/O	Reserved. Always read as 00h.

5.2.5 TDM Interface and Clock Interface Registers

Table 47 - TDM Interface Control Register

Address: 6000 (Hex) **Label: TDMCNT** **Reset Value: 0000 (Hex)**			
Label	**Bit Position**	**Type**	**Description**
TIENA	0	R/W	TDM to/from Internal Memory Process Enable. ‘0’=Disabled; ‘1’=Enabled.
IEENA	1	R/W	Internal to/from External Memory Process Enable. ‘0’=Disabled; ‘1’=Enabled.
GENOE	2	R/W	General Output Enable. Enables TDM data outputs. ‘0’ = TDM data output pins tristated and TDM output (i.e. receive) data is looped back as TDM input (i.e. transmit) data; ‘1’ = Normal TDM operation. In order to prevent collisions on the TDM bus, one should clear all of the Output Enable Registers (addresses 7000 + 2N) prior to setting this bit. When LOW, disables CFAIL and CABS bits in the TDM Interface Status Register (6002h).
CLK_LOOPBACK	3	R/W	TDM Clock Loopback. ‘0’ = Normal operation; ‘1’ = Loopback. In loopback the CLKx2, CLKx1, and FSYNC input signals are replaced by the internally generated clocks, but the clock pins are not driven by the MT90500.
CABSIE	4	R/W	Clock Absent Interrupt Enable. ‘0’=Disabled; ‘1’=Enabled. When enabled, a ‘1’ on CABS in Register 6002h will force a ‘1’ on TDM_SERV in Register 0002h.
CFAILIE	5	R/W	Clock Fail Interrupt Enable. ‘0’=Disabled; ‘1’=Enabled. When enabled, a ‘1’ on CFAIL in Register 6002h will force a ‘1’ on TDM_SERV in Register 0002h.
TOBIE	6	R/W	TDM Out of Bandwidth Interrupt Enable. ‘0’=Disabled; ‘1’=Enabled. When enabled, a ‘1’ on TOB in Register 6002h will force a ‘1’ on TDM_SERV in Register 0002h.
TRUEIE	7	R/W	TDM Read Underrun Error Interrupt Enable. ‘0’=Disabled; ‘1’=Enabled. When enabled, a ‘1’ on TRUE in Register 6002h will force a ‘1’ on TDM_SERV in Register 0002h.
TRUCRIE	8	R/W	TDM Read Underrun Counter Rollover Interrupt Enable. ‘0’=Disabled; ‘1’=Enabled. When enabled, a ‘1’ on TRUCR in Register 6002h will force a ‘1’ on TDM_SERV in Register 0002h.
Reserved	14:9	R/O	Reserved. Always read as “000_000”.
TESTS	15	R/W	TEST Status. Forces all status events in both the TDM Interface Status Register (6002h) and the Clock Module General Status Register (6082h) to occur. Also causes the TDM Read Underrun Count Register (6048h) to be incremented and the TDM Read Underrun Address Register (6046h) to be updated. Used for test purposes only.

Table 48 - TDM Interface Status Register

Address: 6002 (Hex) **Label: TIS** **Reset Value: XX00**			
Label	**Bit Position**	**Type**	**Description**
Reserved	3:0	R/O	Reserved. Always read as “0000”.
CABS	4	R/O/L	Clock Absent. This flag is raised when one or more of the three TDM clock pins (CLKX2, CLKX1, and FSYNC) has not changed state within a specified number of MCLK cycles. The signals are monitored when the pins are inputs (TDM Clock Slave or Clock Master Alternate modes), and also when the pins are outputs (TDM Clock Master mode). This flag is disabled when GENOE is LOW. Writing a ‘1’ over this bit clears it.

Table 48 - TDM Interface Status Register

Address: 6002 (Hex)
Label: TIS
Reset Value: XX00

Label	Bit Position	Type	Description
CFAIL	5	R/O/L	SCSA Clock Fail. This flag is used only when the MT90500 is NOT the clock master (i.e. configured as Slave or as Clock Master Alternate in SCSA mode). This flag is raised and latched when the CLKFAIL pin is sampled HIGH and the CORSIGA pin is configured as CLKFAIL input (i.e. CORSIGACNF in 6004h must be “11”). The CORSIGA bit in this register can be used to verify the current state of the CLKFAIL signal. When this bit is HIGH, and the CLK_ALT bit in 6010h is HIGH, the MT90500 will drive the TDM clock lines (switch from Master Alternate to Master) and if CORSIGACNF is “11”, drive 0 out on CORSIGA/CLKFAIL. This flag is disabled when GENOE is LOW. Writing a ‘1’ over this bit clears it.
TOB	6	R/O/L	TDM Out of Bandwidth. This flag is raised when the internal to/from external memory process is unable to transfer all the data in the specified time. This flag generally indicates that there is a bandwidth limitation in accesses to external memory. External memory access requirements must be reduced, or external memory speed must be increased. The IEENA bit in the TDM Interface Control Register at 6000h must be set for this error to be generated. Writing a ‘1’ over this bit clears it.
TRUE	7	R/O/L	TDM Read Underrun Error. ‘0’ = Error has not occurred. ‘1’ = An underrun has occurred. Indicates the occurrence of an underrun on a TDM read from one of the Receive Circular Buffers. This error-indication is controlled by the TDM Read Underrun Detection Enable (U) bits in the External Memory to Internal TDM Memory Control Structure (i.e. if the U bits are LOW, no underrun errors will be noted in this register). Writing a ‘1’ over this bit clears it.
TRUCR	8	R/O/L	TDM Read Underrun Count Rollover. This flag is raised when the underrun counter at register 6048h returns to 0000h. Writing a ‘1’ over this bit clears it.
TDMSERV	9	R/O	TDM Service Bit. This bit is set if any of the above status bits<8:4> is set.
Reserved	10	R/O	Reserved. Always read as ‘0’.
CORSIGA	11	R/O	CORSIGA pin’s current logic level. Undefined at reset.
CORSIGB	12	R/O	CORSIGB pin’s current logic level. Undefined at reset.
CORSIGC	13	R/O	CORSIGC pin’s current logic level. Undefined at reset.
CORSIGD	14	R/O	CORSIGD pin’s current logic level. Undefined at reset.
CORSIGE	15	R/O	CORSIGE pin’s current logic level. Undefined at reset.

Table 49 - TDM I/O Register

Address: 6004 (Hex)
Label: CORSIG
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CORSIGACNF	1:0	R/W	CORSIGA Configuration. Selects operation of the CORSIGA pin. “00” General I/O pin configured as input (see CORSIGA bit in register 6002h) “01” General I/O pin configured as programmable output (see CORSIGA bit in this register) “10” Reserved “11” CLKFAIL I/O (see CFAIL at 6002h) - zero driven out when the MT90500 is clock master; CLKFAIL input from SCSA bus when in slave mode or inactive clock master alternate.
CORSIGBCNF	3:2	R/W	CORSIGB Configuration. “00” General I/O pin configured as input “01” General I/O pin configured as programmable output (see CORSIGB bit in this register) “10” MC: I/O for SCSA message channel (RXDATA sent to CORSIGD; TXDATA read from CORSIGC “11” Reserved.
CORSIGCCNF	5:4	R/W	CORSIGC Configuration. “00” General I/O pin configured as input “01” General I/O pin configured as programmable output (see CORSIGC bit in this register) “10” HDLC MCTX: data input for SCSA message channel “11” Reserved.
CORSIGDCNF	7:6	R/W	CORSIGD Configuration. “00” General I/O pin configured as input “01” General I/O pin configured as programmable output (see CORSIGD bit in this register) “10” HDLC MCRX: data output for SCSA message channel “11” Reserved.
CORSIGECNF	9:8	R/W	CORSIGE Configuration. “00” General I/O pin configured as input “01” General I/O pin configured as programmable output (see CORSIGE bit in this register) “10” HDLC MCCLK: clock output for SCSA message channel “11” Reserved.
Reserved	10	R/W	Reserved. Should be set to ‘0’.
CORSIGA	11	R/W	Value that will be driven on CORSIGA output pin (only applicable if CORSIGACNF=“01”).
CORSIGB	12	R/W	Value that will be driven on CORSIGB output pin (only applicable if CORSIGBCNF=“01”).
CORSIGC	13	R/W	Value that will be driven on CORSIGC output pin (only applicable if CORSIGCCNF=“01”).
CORSIGD	14	R/W	Value that will be driven on CORSIGD output pin (only applicable if CORSIGDCNF=“01”).
CORSIGE	15	R/W	Value that will be driven on CORSIGE output pin (only applicable if CORSIGECNF=“01”).

Table 50 - TDM Bus Type Register

Address: 6010 (Hex)
Label: TDMTYP
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDMFS	1:0	R/W	TDM Fsync type. “00” = negative polarity for half-cycle of CLKx1, straddling the frame boundary (SCSA/ MVIP/H-MVIP/ST-BUS); “01” = Reserved; “10” = Reserved; “11” = positive polarity for full-cycle of CLKx1, preceding the frame boundary (IDL). When using the positive polarity frame sync, TCLKSYN (bit<6>) must be LOW, and the SC bus HDLC access will not function (pins MC, MCRX, MCTX and MCCLK).
TDMSMPL	3:2	R/W	TDM Sampling. Determines the sampling point of the serial input bit. “00” = 4/4; “01” = 3/4; “10” = 2/4; “11” = Reserved.
TDMCLK	5:4	R/W	TDM Clock speed. Determines the data rate of the TDM bus (and CLKX1). “00” = 2 MHz, 32 time slots/frame; “01” = 4 MHz, 64 time slots/frame; “10” = 8 MHz, 128 time slots/frame; ”11” = Reserved.
TCLKSYN	6	R/W	Selects source for internal CLKx1. ‘0’ = use CLKx1 input buffer (normal operation, TDM Slave and Master); ‘1’ = derive CLKx1 from CLKx2 (Slave mode where no CLKx1 is provided by TDM bus) In TDM Slave mode, if the CLKx1 pin is not used as an input it remains high-impedance.
CLKTYPE	7	R/W	Clock Type. Selects operation of CLKx2 Input when TDM Slave mode is selected (no effect when TDM Master mode is selected). ‘0’ = single-ended input (one input pin: CLKx2); ‘1’ = differential input (two input pins: CLKx2PI and CLKx2NI).
CLKMASTER	8	R/W	TDM Clock Master. ‘0’ = MT90500 is TDM Slave, and does not drive TDM clock pins (CLKx2 is an input); ‘1’ = MT90500 is TDM Master, and drives the TDM clock pins (MT90500 drives CLKx2, CLKx1, and FSYNC).
CLKALT	9	R/W	TDM Clock Alternate. ‘0’ = disabled; ‘1’ = MT90500 is designated as Clock Master Alternate The Clock Master Alternate will become the Clock Master and drive the clock lines only if the clock fail status bit (CFAIL in 6002h) is HIGH. **Note**: This bit is only used when CORSIGACNF in 6004h is “11”, indicating that the CORSIGA pin is configured as CLKFAIL input (SCSA mode).
Reserved	10	R/W	Reserved. Must always be set to ‘0’.
BUSHOLD	11	R/W	BUS Hold Time. ‘0’ = fast bus (SCSA 8 Mbps); ‘1’ = slow bus (MVIP / SCSA2 / IDL / ST-BUS)
Reserved	15:12	R/O	Reserved. Always read as “0000”.

Table 51 - Local Bus Type Register

Address: 6020 (Hex)
Label: LBTYP
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
LBUSFS	1:0	R/W	Local Bus Fsync type. “00” = negative polarity for half-cycle of LOCx1, straddling the frame boundary (SCSA/ MVIP/H-MVIP/ST-BUS); “01” = Reserved; “10” = Reserved; “11” = positive polarity for full-cycle of LOCx1, preceding the frame boundary (IDL).
LBUSSMPL	3:2	R/W	Local Bus Sampling. “00” = 4/4; “01” = 3/4; “10” = 2/4; “11” = Reserved.
Reserved	5:4	R/W	Reserved. Should be written as “00”.
LCLKDIV	7:6	R/W	Local Bus Clock Division factor. Amount that TDM backplane clock must be divided to generate 2.048 Mbps local bus. “00” = Direct; “01” = Divided by 2; “10” = Divided by 4; “11” = Reserved.
STi2LOCSTo	11:8	R/W	Indicates which input TDM stream will be routed to LOCSTo.
LOCSTi2STo	15:12	R/W	Indicates on which output TDM stream LOCSTi will be routed.

Table 52 - TDM Bus to Local Bus Transfer Register

Address: 6022 (Hex)
Label: TDMLOC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TDM2LOCTS	6:0	R/W	LOCSTo TDM Time Slot. Input TDM time slot which will be transmitted out on LOCSTo time slot 0.
Reserved	7	R/W	Reserved. Should be written as ‘0’.
LOCSToNUM	14:8	R/W	LOCSTo Number of Time Slots. Number of time slots that are passed from the TDM bus to the local bus. “0000000” = 1 channel; “0011111” = 32 channels.
TENA	15	R/W	Transfer Enable. When ‘0’, the transfer process from the TDM bus to the local bus is disabled. When ‘1’, the transfer is enabled. Whenever the transfer of data from the TDM bus to the local bus is disabled (either because this bit is ‘0’ or because the specified number of time slots has been transferred), LOCSTi and LOCSTo are internally connected and operate in loopback mode.

Table 53 - Local Bus to TDM Bus Transfer Register

Address: 6024 (Hex)
Label: LOCTDM
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
LOC2TDMTS	6:0	R/W	LOCSTi TDM Time Slot. Output TDM time slot on which LOCSTi time slot 0 will be transmitted.
Reserved	7	R/W	Reserved. Should be written as ‘0’.
LOCSTiNUM	14:8	R/W	LOCSTi Number of Time Slots. Number of time slots that are passed to the TDM bus from the local bus. “0000000” = 1 channel; “0011111” = 32 channels.
RENA	15	R/W	Receive Enable. When '1', the transfer process is enabled and from 1 to 32 local bus time slots will replace the TDM data coming from the RX_SAR. **Note:** The Output Enable Registers must be enabled to permit these data bytes to be transferred out on the TDM bus.

Table 54 - TX Circular Buffer Control Structure Base Register

Address: 6040 (Hex)
Label: TXCBCS
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TXCBCSL	3:0	R/W	TX Circular Buffer Control Structure Length. “0000” = 128 entries; “0001” = 256 entries; “0010” = 512 entries; “0011” = 1024 entries; “0100” = 2048 entries; other = reserved.
TXCBCSBASE	15:4	R/W	TX Circular Buffer Control Structure Base Address. This field represents bits<20:9> of the base address of the TX Circular Buffer Control Structure. The table that this structure points to must not cross an 8 Kbyte boundary.
Refer to Figure 5 on page 32 for implementation details.			

Table 55 - External to Internal Memory Control Structure Base Register

Address: 6042 (Hex)
Label: EIMM
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
EIMCSL	3:0	R/W	External to Internal Memory Control Structure Length. “0000” = 128 entries; “0001” = 256 entries; “0010” = 512 entries; “0011” = 1024 entries; “0100” = 2048 entries; other = reserved.
EIMCSBASE	15:4	R/W	External to Internal Memory Control Structure Base Address. This field represents bits<20:9> of the base address of the External to Internal Memory Control Structure. The table that this structure points to must not cross an 8 Kbyte boundary.
Refer to Figure 7 on page 35 for implementation details.			

Table 56 - TX Circular Buffer Base Address Register

Address: 6044(Hex)
Label: TXCBBA
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Reserved	3:0	R/W	Reserved. Should be written as “0000”.
TXCBBASE	15:4	R/W	TX Circular Buffer Base Address. This field represents bits<20:9> of the base address of the TX Circular Buffer’s base address. The pointer to the circular buffers must not overlap a 64 Kbyte boundary.

Table 57 - TDM Read Underrun Address Register

Address: 6046 (Hex)
Label: RXUNDA
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TRURTSST	10:0	R/O	TDM Read Underrun Time Slot Stream. Contains the time slot (bits<10:4>) and stream (bits<3:0>) on which the last underrun was detected.
Reserved	15:11	R/O	Reserved, always read as “0000_0”.

Table 58 - TDM Read Underrun Count Register

Address: 6048 (Hex)
Label: RXUNDC
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
TRURCOUNT	15:0	R/O	TDM Read Underrun Counter. Each time a TDM read underrun occurs, this register’s value is incremented.

Table 59 - Clock Module General Control Register

Address: 6080 (Hex)
Label: CMGCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
REFFAILIE	0	R/W	REFFAIL Interrupt Enable - Clock Generation Sub-Module. When enabled, a ‘1’ on REFFAIL in Register 6082h will force a ‘1’ on TIM_SERV in Register 0002h.
SRTSTSIE	1	R/W	Write ‘0’.
CNTUPDATE	2	R/W	Counter Update Control - When a ‘1’ is written to this bit, the counts in registers 0x60A2, 0x60A4, and 0x60A6 are updated. The values in those registers will remain the same until the next time a ‘1’ is written to this bit. The static value of this bit is always ignored.
SRTSRSIE	3	R/W	Write ‘0’.
Reserved	4	R/W	Reserved. Should be written as ‘0’.
LOSSCIE	5	R/W	Loss of Timing Reference Cells Interrupt Enable - Timing Reference Cell Sub-Module. When enabled, a ‘1’ on LOSS_TIMF in Register 6082h will force a ‘1’ on TIM_SERV in Register 0002h.
OUT_SYNC_IE	6	R/W	Out-Of-Sync Interrupt Enable - Timing Reference Cell Sub-Module. When enabled, a ‘1’ on OUT_SYNC in Register 6082h will force a ‘1’ on TIM_SERV in Register 0002h.
TIM_ENA	7	R/W	Timing Enable - When ‘1’, enables the operation of the Timing Reference Cell Sub-Module receive circuit for Adaptive Clock Recovery.
Reserved	15:8	R/O	Will always read 00h.

Table 60 - Clock Module General Status Register

Address: 6082 (Hex)
Label: CMGSR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
REFFAIL	0	R/O/L	Reference Clock Failure - Clock Generation Sub-Module. When '1', indicates that the REF8KCLK signal has failed. When this bit is '1' and the FREERUN bits in the Master Clock Generation Control Register (MCGCR at 6090h) are "01", the external signal FREERUN will be activated. **MCLK should be at least 2048 times the REF8KCLK frequency for proper operation.** Writing a '1' over this bit will clear it.
SRTST_UND	1	R/O/L	Can be ignored.
SRTST_OVR	2	R/O/L	Can be ignored.
SRTSR_UND	3	R/O/L	Can be ignored.
SRTSR_OVR	4	R/O/L	Can be ignored.
LOSS_TIMRF	5	R/O/L	Loss of Timing Reference Cell stream - Timing Reference Cell Sub-Module. When '1', indicates a loss of timing reference cells (or marker) event has occurred (loss period determined by Time-out field at 60A0h) while the Adaptive Clock Recovery state machine was enabled (TIM_ENA bit set in Clock Module General Control Register at 6080h). Writing a '1' over this bit will clear it.
OUT_SYNC	6	R/O/L	Out-Of-Sync - Timing Reference Cell Sub-Module. When '1', indicates the Timing Reference Cell state machine went out of sync. **This bit is set only when the state machine initially goes out of sync - if it stays out of sync., this bit will be cleared.** Writing a '1' over this bit will clear it.
Reserved	14:7	R/O	Will always read "000_0000_0".
TIME_SERV	15	R/O	This bit is set if any of bits<6:0> are set.

Note: Bits<6:0> will be set if the TESTS bit is set in the TDM Interface Control Register at 6000h.

Table 61 - Master Clock Generation Control Register

Address: 6090 (Hex)
Label: MCGCR
Reset Value: 00C0 (Hex)

Label	Bit Position	Type	Description
REFSEL	1:0	R/W	REF8KCLK (8 kHz Reference Clock) Selection. See Figure 3 on page 27. 00 -> MCLK/(DIVCLK + 2) or CLKx2/(DIVCLK + 2) (See register 6092h.) 01 -> RXVCLK (recovered ATM VC/SW clock. See register 60A8h.) 10 -> SEC8K input pin 11 -> EX_8KA input pin.
DIVCLK_SRC	2	R/W	Selects input clock for programmable divider (See register 6092h.) 0 -> MCLK 1 -> CLKx2
EX_8KA_SQ	3	R/W	Select squared version of EX_8KA for output. 0 -> Pass EX_8KA signal without changes, 1 -> Convert EX_8KA input to square wave. This bit, when HIGH, selects the squared version of EX_8KA for routing to the REF8KCLK, and the SEK8K multiplexers. The squaring logic converts the EX_8KA input into a square wave (approximately 50% duty-cycle). This can convert a pulse 8 kHz signal into an 8 kHz square wave, for example. The rising edge of EX_8KA input is passed, without added jitter, to the REF8KCLK or SEC8K output as a falling edge (i.e. the signal is inverted); the rising edge at the REF8KCLK output will be 50% duty cycle with jitter equal to a cycle of MCLK. MCLK must be at least 10 times faster, and at most 16000 times faster, than EX_8KA. See Figure 3, "TDM Clock Selection and Generation Logic," on page 27.

Table 61 - Master Clock Generation Control Register

Address: 6090 (Hex)
Label: MCGCR
Reset Value: 00C0 (Hex)

Label	Bit Position	Type	Description
SEC8K_SQ	4	R/W	Enable SEC8K squaring logic. 0 -> Pass SEC8K signal without changes, 1 -> Convert SEC8K input to square wave. The squaring logic, when enabled, converts the SEC8K input into a square wave (approximately 50% duty-cycle) before passing it to the REF8KCLK multiplexer. This can convert a pulse 8 kHz signal into an 8 kHz square wave, for example. When REFSEL = “10” the rising edge of SEC8K input is passed, without added jitter, to the REF8KCLK output as a rising edge; the falling edge at the REF8KCLK output will be 50% duty cycle with jitter equal to a cycle of MCLK. MCLK must be at least 10 times faster, and at most 16000 times faster, than SEC8K.
BEPLL	5	R/W	Clock Generator Multiplexer Selection: selects **CLK16** input clock for the TDM Clock Generator. 0 -> MCLK 1 -> PLLCLK input.
DIV1...8	7:6	R/W	Clock Generator Division Factor. (“11” at reset) 00 -> 8 01 -> 1 10 -> 2 11 -> 4 **Note:** These bits provide the factor by which either MCLK or PLLCLK (as determined by BEPLL) is divided to provide a 16.384 MHz clock at the Main TDM Bus Clock Generation Logic.
PHLEN	8	R/W	Clock Generator Phase Lock Enable. When this bit is ‘1’, and TDMFS (in the TDM Bus Type Register at 6010h) is “00”, the internal FSYNC signal generator will be slaved to the external FSYNC signal. This bit allows the MT90500 to be used as a Clock Master Alternate in SCSA mode (i.e. CLKALT = ‘1’ and CLKMASTER = ‘0’ in TDM Bus Type Register at 6010h). In this case, the stand-by clock master circuit (using CLK16, the local 16.384 MHz clock derived from PLLCLK or MCLK) tracks the external FSYNC signal so that when it is selected as a clock master after a clock failure, the new FSYNC will be almost in phase with the previous one. **The phase-tracking is automatically disabled when the CLKFAIL input pin is asserted.**
SEC8KEN	9	R/W	When ‘1’, the MT90500 drives the SEC8K external signal. When ‘0’, the SEC8K pin is an input.
SEC8KSEL	10	R/W	SEC8K Clock Source Selection 0 -> EX_8KA 1 -> Internally generated 8 kHz reference (**FS_INT**)
FREERUN	12:11	R/W	Clock Failure Detection - FREERUN Signal Control 00 -> FREERUN is always activated (FREERUN pin is HIGH) 01 -> FREERUN is activated when status bit REFFAIL (in the Clock Module General Status Register at 6082h) is ‘1’. In the event of REF8KCLK clock failure, it is the software’s responsibility to change the programming from “01” to “00” before clearing the REFFAIL status bit. 1X -> FREERUN is always deactivated (FREERUN pin is LOW)
Reserved	15:13	R/W	Reserved. Should be written as “000”.

Refer to Figure 3, “TDM Clock Selection and Generation Logic,” on page 27 for more detailed information regarding the implementation of the selection bits.

Table 62 - Master Clock / CLKx2 Division Factor

Address: 6092 (Hex)
Label: MCDF
Reset Value: 2000 (Hex)

Label	Bit Position	Type	Description
DIVCLK	13:0	R/W	This value plus two is used to divide MCLK or CLKx2 to get an 8 kHz reference. Value 0000h means divide-by-two, 0001h means divide-by-three, ..., 3FFEh means divide-by-16,384.
Reserved	15:14	R/W	Reserved. Should be written as “00”.

Table 63 - Timing Reference Processing Control Register

Address: 60A0 (Hex)
Label: TRPCR
Reset Value: 0001 (Hex)

Label	Bit Position	Type	Description
Time-out	9:0	R/W	This value is used to indicate a time-out period, after which if no timing reference cells or markers have been received, a Loss of Timing Reference Cells (LOSS_TIMRF in 6082h) event will be indicated. The time-out period is calculated in multiples of 65536 MCLK periods. “00_0000_0000” is an illegal value (i.e. time-out is a minimum of 65536 cycles of MCLK).
Cell / 8 kHz	10	R/W	When ‘0’, indicates that clock recovery is based on Timing Reference Cell arrival events. When ‘1’, indicates that clock recovery is based on 8 kHz marker arrival events.
Seq_CRC_Ena	11	R/W	When ‘1’, enable CRC and parity checking on AAL1 sequence number field in state machine. See Figure 31 on page 65.
Reserved	15:12	R/W	Reserved. Should be written as “0000”.

Table 64 - Event Count Register

Address: 60A2 (Hex)
Label: EVCR
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
Event_Cnt	15:0	R/O	This register keeps a running count of the reception of timing reference cells or 8 kHz markers (as determined by setting of Cell / 8 kHz bit in register 60A0h). The contents of this register are locked when a ‘1’ is written to the CNTUPDATE bit in the Clock Module General Control Register (6080h). Thus CNTUPDATE should be set just prior to reading this register. See Figure 31, “Adaptive Clock Recovery Sub-Module (Simplified Functional Block Diagram),” on page 65 for more details.

Table 65 - CLKx1 Count - Low Register

Address: 60A4 (Hex)
Label: C1CRL
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CLKx1_Cnt_L	15:0	R/O	This register represents the low portion of a 24-bit counter which keeps a running count of CLKx1 * 8 periods (i.e. every 8 cycles of CLKx1, a counter is incremented). The counter is updated at the same time the Event Count Register (60A2h) is incremented. The contents of this register are locked when a ‘1’ is written to the CNTUPDATE bit in the Clock Module General Control Register (6080h). This should be done just prior to reading this register. See Figure 31, “Adaptive Clock Recovery Sub-Module (Simplified Functional Block Diagram),” on page 65 for more details.

Table 66 - CLKx1 Count - High Register

Address: 60A6 (Hex)
Label: C1CRH
Reset Value: 0000 (Hex)

Label	Bit Position	Type	Description
CLKx1_Cnt_H	7:0	R/O	This register represents the high portion of a 24-bit counter which keeps a running count of CLKx1 * 8 periods (i.e. every 8 cycles of CLKx1, a counter is incremented). The counter is updated at the same time the Event Count Register (60A2h) is incremented. The contents of this register are locked when a '1' is written to the CNTUPDATE bit in the Clock Module General Control Register (6080h). This should be done just prior to reading this register. See Figure 31, "Adaptive Clock Recovery Sub-Module (Simplified Functional Block Diagram)," on page 65 for more details.
Reserved	15:8	R/O	Unused. Always read 00h.

Table 67 - DIVX Register

Address: 60A8 (Hex)
Label: DIVX
Reset Value: 2000 (Hex)

Label	Bit Position	Type	Description
DIVX	13:0	R/W	This value is used (along with DIVXN, in the next register) to divide MCLK to obtain an RXVCLK reference. The average frequency of RXVCLK is obtained as follows: $$RXVCLKavg = MCLK \times \frac{1}{\frac{(DIVX+2)(DIVXN)+(DIVX+3)\times(4096-DIVXN)}{4096}}$$
Reserved	15:14	R/W	Reserved. Should be written as "00".

Table 68 - DIVX Ratio Register

Address: 60AA (Hex)
Label: DIVXR
Reset Value: 0FFF (Hex)

Label	Bit Position	Type	Description
DIVXN	11:0	R/W	This value defines how many times MCLK will be divided by (DIVX + 2) and how many times it will be divided by (DIVX + 3), as per the formula shown in 60A8h above. When 001h, MCLK is divided by (DIVX + 2) once, then divided 4095 times by (DIVX + 3). Note: 0 is an illegal value for DIVXN (same ratio as 1)
Reserved	15:12	R/W	Reserved. Should be written as "0000".

5.2.6 TDM Time Slot Control

Table 69 - Output Enable Registers

Address: 7000 + 2N (Hex) - N=0,1,2,...,127
Label: OEM
Reset Value: XXXX (Hex)

Label	Bit Position	Type	Description
OE	15:0	R/W	Output Enable for 16 time slots - When HIGH, these bits enable the corresponding time slots to be driven onto the TDM bus. <0> OE for stream 0 <1> OE for stream 1 <2> OE for stream 2 ..... <14> OE for stream 14 <15> OE for stream 15
Each register represents a particular time slot (e.g. 7000h => time slot 0; 70FEh => time slot 127). Within each register, the individual bits correspond to the ST-BUS streams, as listed above.			

6. Electrical Specification

6.1 DC Characteristics

Table 70 - Absolute Maximum Ratings

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage - 5 Volt Rail	V_{DD5}	- 0.3	6.5	V
2	Supply Voltage - 3.3 Volt Rail	V_{DD3}	- 0.3	3.9	V
3	Voltage on any I/O pin (except $\overline{\text{TRISTATE}}$)	$V_{I/O}$	V_{SS} - 0.5	V_{DD5} + 0.3	V
4	Voltage on $\overline{\text{TRISTATE}}$ pin	$V_{I/O3}$	V_{SS} - 0.5	V_{DD3} + 0.3	V
5	Continuous current at digital inputs	I_{IN}		±10	mA
6	Continuous current at digital outputs	I_O		± 24	mA
7	Storage Temperature	T_S	- 40	+ 125	°C
8	Package power dissipation (PQFP)	PD		4	W

* Exceeding these figures may cause permanent damage. Functional operation under these conditions is not guaranteed.
Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

Table 71 - Recommended Operating Conditions

	Characteristics	Sym	Min	Typ[a]	Max	Units	Test Conditions
1	Operating Temperature	T_{OP}	- 40		+ 85	°C	
2	Supply Voltage, 5 Volt Rail	V_{DD5}	4.75	5.0	5.25	V	
3	Supply Voltage, 3.3 Volt Rail	V_{DD3}	3.0	3.3	3.6	V	
4	Input Voltage High - TTL & 3V CMOS inputs		2.4		V_{DD5}	V	
5	Input Voltage Low - all inputs		V_{SS}		0.4	V	
6	Input Voltage High - $\overline{\text{TRISTATE}}$ input		2.4		3.6	V	V_{DD3} = 3.3 V

a. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

Table 72 - DC Characteristics

	Characteristics	Sym	Min	Typ[a]	Max	Units	Test Conditions [b]
1	Supply Current - 3.3 V supply	I_{DD3}		400	500	mA	60 MHz, Outputs unloaded
2	Supply Current - 5 V supply	I_{DD5}		1		mA	Outputs unloaded
3	Input High Voltage (3V CMOS)	V_{IHC}	0.7 x V_{DD3}	2.3		V	
4	Input Low Voltage (3V CMOS)	V_{ILC}		0.7	0.2 x V_{DD3}	V	
5	Switching Threshold (3V CMOS)	V_{TC}		0.5 x V_{DD3}		V	
6	Input High Voltage (TTL)	V_{IH}	2.0		5.5	V	
7	Input Low Voltage (TTL)	V_{IL}	V_{SS} - 0.5		0.8	V	
8	Switching Threshold (TTL)	V_{TT}		1.4	2.0	V	
9	Schmitt Trigger Positive Threshold	V_{t+}		1.7	2.0	V	
10	Schmitt Trigger Negative Threshold	V_{t-}	0.8	1.0		V	
11	Schmitt Trigger Hysteresis	V_{tH}	0.6	0.7		V	
12	Differential Input High Voltage	V_{IHD}		+ 0.5		V	CLKx2PI - CLKx2NI

Table 72 - DC Characteristics

	Characteristics	Sym	Min	Typ[a]	Max	Units	Test Conditions [b]
13	Differential Input Low Voltage	V_{ILD}		- 0.5		V	CLKx2PI - CLKx2NI
14	Input Leakage Current	I_{IL} / I_{IH}		± 1	± 10	µA	V_{IN} = V_{DDx} or V_{ss}
	Inputs with pull-down resistors	I_{IH}	69	124	190	µA	V_{IN} = V_{DD5}
	Inputs with pull-up resistors	I_{IL}	- 70	- 142	- 225	µA	V_{IN} = V_{ss}
15	Input Pin Capacitance	C_I			10	pF	
16	Output HIGH Voltage	V_{OH}	2.4	3.3	V_{DDX}	V	I_{OH} = rated current (4 or 12 mA)
17	Output LOW Voltage	V_{OL}		0.2	0.4	V	I_{OL} = rated current (4 or 12 mA)
18	High Impedance Leakage	I_{OZ}	-10	±1.0	+10	µA	V_O = V_{SS} or V_{DD}
19	Output Pin Capacitance	C_O			10	pF	

a. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
b. T_{OP} = -40°C to 85°C; V_{DD5} = 5V ± 5%; V_{DD3} = 3.3V ± 5%
Voltage measurements are with respect to ground (V_{SS}) unless otherwise stated.

Precautions During Power Sequencing

Latch-up is not a concern during power sequencing. There is no requirement for sequencing 3.3 V and 5 V supplies during power up. However, to minimize over-voltage stress during system start-up, the 3.3 V supply applied to the MT90500 should be brought to a level of at least VDD = 3.0 V before a signal line is driven to a level greater than or equal to 3.3 V. This practice can be implemented either by ensuring that the 3.3 V power turns on simultaneously with or before the system 5 V supply turns on, or by ensuring that all 5 V signals are held to a logic LOW state during the time that VDD < 3.0 V. Regardless of the method chosen to limit over-voltage stress during power up, exposure must be limited to no more than + 6.5 V input voltage (V_{IN}). The $\overline{\text{TRISTATE}}$ pin of the MT90500 can be asserted low on power-up to prevent bus contention.

Precautions During Power Failure

Latch-up is not a concern in power failure mode. Although extended exposure of the MT90500 to 5 V signals during 3.3 V supply power failure is not recommended, there are no restrictions as long as V_{IN} does not exceed the absolute maximum rating of 6.5 V. To minimize over-voltage stress during a 3.3 V power supply failure, the designer should either link the power supplies to prevent this condition or ensure that all 5 V signals connected to the MT90500 are held in a logic LOW state until the 5 V supply is deactivated.

Pull-ups

Pull-ups from the 5V rail to 3.3V (5V tolerant) outputs of the MT90500 can cause reverse leakage currents into those 3.3V outputs when they are active HIGH. (No significant reverse current is present during the high impedance state.) If the application can put the MT90500 in a state where MCLK is stopped, and a large number of 3.3V output buffers are held in a static HIGH state, current can flow from the 5V rail to the 3.3V rail. If this MCLK-stopped state can not be avoided, the user should determine if the total MT90500 reverse current will have a negative impact on the system 3.3V power supply. Alternatively, the $\overline{\text{TRISTATE}}$ pin of the MT90500 can be asserted low to put all outputs in the high impedance state.

6.2 AC Characteristics

6.2.1 Main TDM Bus

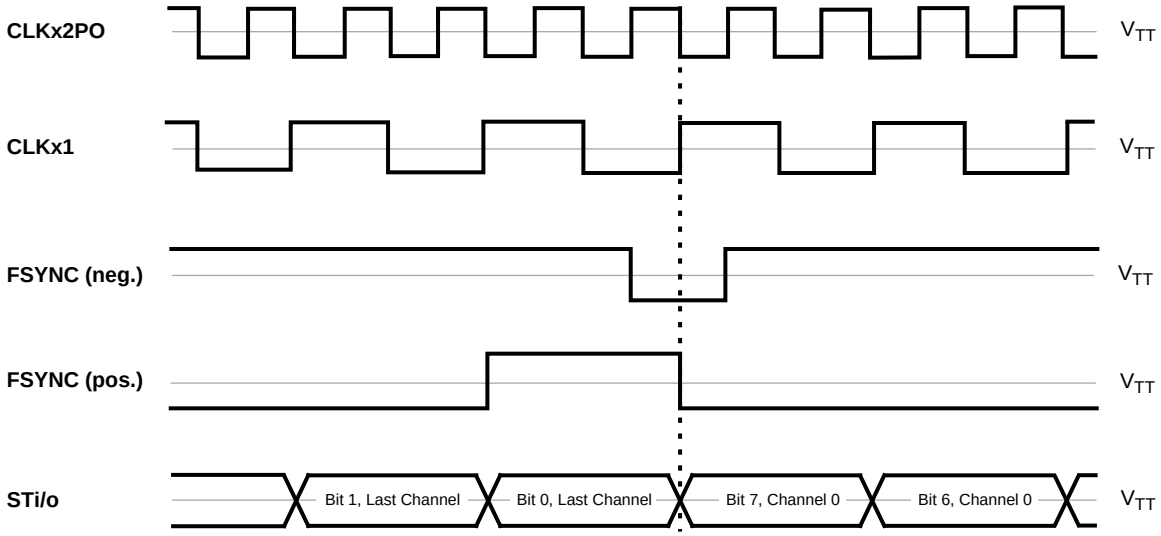


Figure 35 - Nominal TDM Bus Timing

Table 73 - Main TDM Bus Output Clock Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Clock Skew - CLKx2PO falling to CLKx1 change	t_{SK}			10	ns	C_L = 50 pF
				20	ns	C_L = 200 pF
CLKx2PO - Output Clock Period	t_{Cx2P}					
2.048 Mbps bus (4.096 MHz clock)			244		ns	
4.096 Mbps bus (8.192 MHz clock)			122		ns	
8.192 Mbps bus (16.384 MHz clock)			61		ns	
CLKx2PO Pulse Width (HIGH / LOW)	$t_{Cx2H/L}$					16.39 MHz (61 ns) input clock with 50/50 duty cycle.
2.048 Mbps bus (4.096 MHz clock)		118	122	126	ns	
4.096 Mbps bus (8.192 MHz clock)		57	61	65	ns	
8.192 Mbps bus (16.384 MHz clock)		26.5	30.5	34.5	ns	
CLKx1 - Output Clock Period	t_{Cx1P}					
2.048 Mbps			488		ns	
4.096 Mbps			244		ns	
8.192 Mbps			122		ns	
CLKx1 Pulse Width (HIGH / LOW)	$t_{Cx1H/L}$					16.39 MHz (61 ns) input clock.
2.048 Mbps		240	244	248	ns	
4.096 Mbps		118	122	126	ns	
8.192 Mbps		57	61	65	ns	
Frame Pulse Width	t_{FPW}					16.39 MHz (61 ns) input clock.
Positive Frame Pulse - 2.048 Mbps			488		ns	
Negative Frame Pulse - 2.048 Mbps			244		ns	
Positive Frame Pulse - 4.096 Mbps			244		ns	
Negative Frame Pulse - 4.096 Mbps			122		ns	
Positive Frame Pulse - 8.192 Mbps			122		ns	
Negative Frame Pulse - 8.192 Mbps			61		ns	
Frame Pulse Delay	t_{FPD}					
Positive: CLKx2PO falling to FSYNC rising		0		10	ns	C_L = 50 pF
		-2		20	ns	C_L = 200 pF
Negative: CLKx2PO rising to FSYNC falling		0		10	ns	C_L = 50 pF
		-2		20	ns	C_L = 200 pF

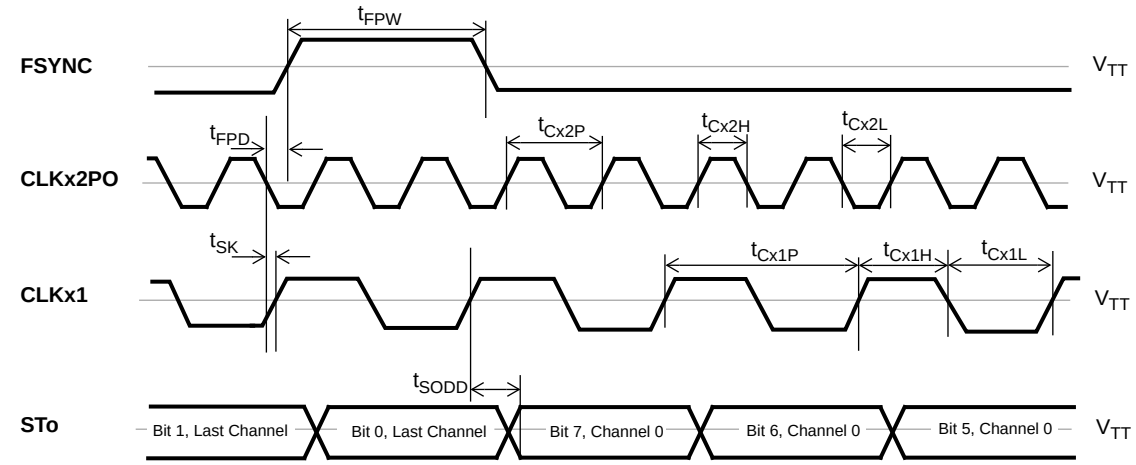


Figure 36 - Main TDM Bus Output Clocking Parameters - Positive Frame Pulse

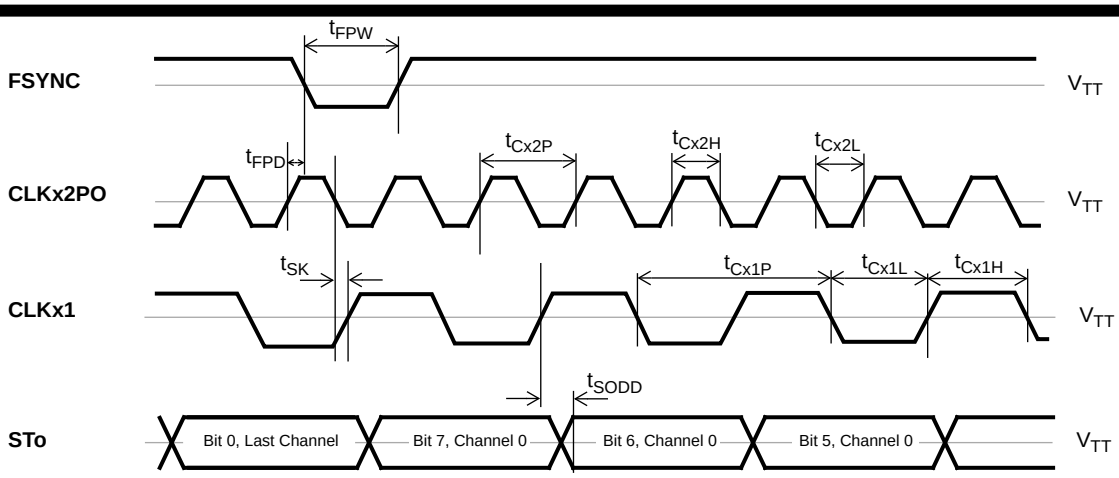


Figure 37 - Main TDM Bus Output Clocking Parameters - Negative Frame Pulse

NOTE: Some SCSA devices may require a wider frame pulse at 4 Mbps and at 8 Mbps than the MT90500 provides. Also, H-MVIP uses a 488 ns wide frame pulse at 8 Mbps.

Table 74 - Main TDM Bus Data Output Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
STo Delay - Data to Data Change CLKx1 rising and (STo HIGH or STo LOW) to STo change	t_{SODX}					
Fast Bus		5			ns	C_L = 50 pF
		10			ns	C_L = 200 pF
Slow Bus		5			ns	C_L = 50 pF
		15			ns	C_L = 200 pF
STo Delay - Data to Data Valid CLKx1 rising and (STo HIGH or STo LOW) to (STo LOW or STo HIGH)	t_{SODD}					
Fast Bus				31	ns	C_L = 50 pF
				41	ns	C_L = 200 pF
Slow Bus				52	ns	C_L = 50 pF
				62	ns	C_L = 200 pF
Drive to High-Z CLKx1 rising and STo VALID to STo HIGH-Z	t_{SODZ}					C_L = 200 pF
Fast Bus				20	ns	
Slow Bus				20	ns	
High-Z to Drive CLKx1 rising and STo HIGH-Z to STo change	t_{SOZX}					C_L = 200 pF
Fast Bus		5			ns	
Slow Bus		10			ns	
High-Z to Data Valid CLKx1 rising and STo HIGH-Z to STo VALID	t_{SOZD}					C_L = 200 pF
Fast Bus				41	ns	
Slow Bus				62	ns	

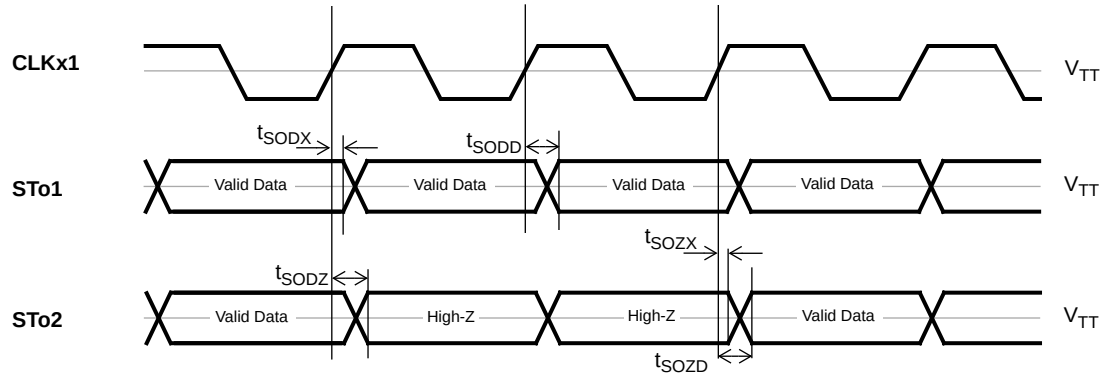


Figure 38 - Main TDM Bus - Serial Output Timing

Table 75 - Main TDM Bus Input Clock Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Clock Skew - CLKx2 falling to CLKx1 change	t_{FSK}			10	ns	
CLKx2 - Input Clock Period	t_{Cx2P}					
2.048 Mbps bus (4.096 MHz clock)			244		ns	
4.096 Mbps bus (8.192 MHz clock)			122		ns	
8.192 Mbps bus (16.384 MHz clock)			61		ns	
CLKx2 Input Pulse Width (HIGH / LOW)	$t_{Cx2H/L}$					16.39 MHz (61 ns) input clock with 50/50 duty cycle.
2.048 Mbps bus (4.096 MHz clock)		97.6	122	146.4	ns	
4.096 Mbps bus (8.192 MHz clock)		48.8	61	73.2	ns	
8.192 Mbps bus (16.384 MHz clock)		26.2	30.5	34.8	ns	
CLKx1 - Input Clock Period	t_{Cx1P}					
2.048 Mbps			488		ns	
4.096 Mbps			244		ns	
8.192 Mbps			122		ns	
CLKx1 Pulse Width (HIGH / LOW)	$t_{Cx1H/L}$					16.39 MHz (61 ns) input clock.
2.048 Mbps		195.2	244	292.8	ns	
4.096 Mbps		97.6	122	146.4	ns	
8.192 Mbps		48.8	61	73.2	ns	
PLLCLK - Input Clock Period	t_{PLL}					
16.384 MHz			61		ns	
PLLCLK Pulse Width (HIGH / LOW)	$t_{PLLH/L}$					
16.384 MHz		26.2	30.5	34.8	ns	
Frame Pulse Setup Time	t_{FIS}					*MT90500* is TDM Timing Bus Slave.
FSYNC valid to CLKx2 falling (TCLKSYN = 1)		5			ns	
FSYNC valid to CLKx1 rising (negative FSYNC)		5				
FSYNC valid to CLKx1 falling (positive FSYNC)		5				
Frame Pulse Hold Time	t_{FIH}					*MT90500* is TDM Timing Bus Slave.
CLKx2 falling to FSYNC invalid (TCLKSYN = 1)		10			ns	
CLKx1 rising to FSYNC invalid (negative FSYNC)		10				
CLKx1 falling to FSYNC invalid (positive FSYNC)		10				

Table 76 - Main TDM Bus Input Data Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
STi Setup Time - STi VALID to CLKx1 falling 2/4 Sampling	t_{SIS}	5			ns	
STi Hold Time - CLKx1 falling to STi INVALID 2/4 Sampling	t_{SIH}	10			ns	
STi Setup Time - STi VALID to CLKx2 rising 3/4 Sampling	t_{SIS}	5			ns	
STi Hold Time - CLKx2 rising to STi INVALID 3/4 Sampling	t_{SIH}	10			ns	
STi Setup Time - STi VALID to CLKx1 rising 4/4 Sampling	t_{SIS}	5			ns	
STi Hold Time - CLKx1 rising to STi INVALID 4/4 Sampling	t_{SIH}	10			ns	

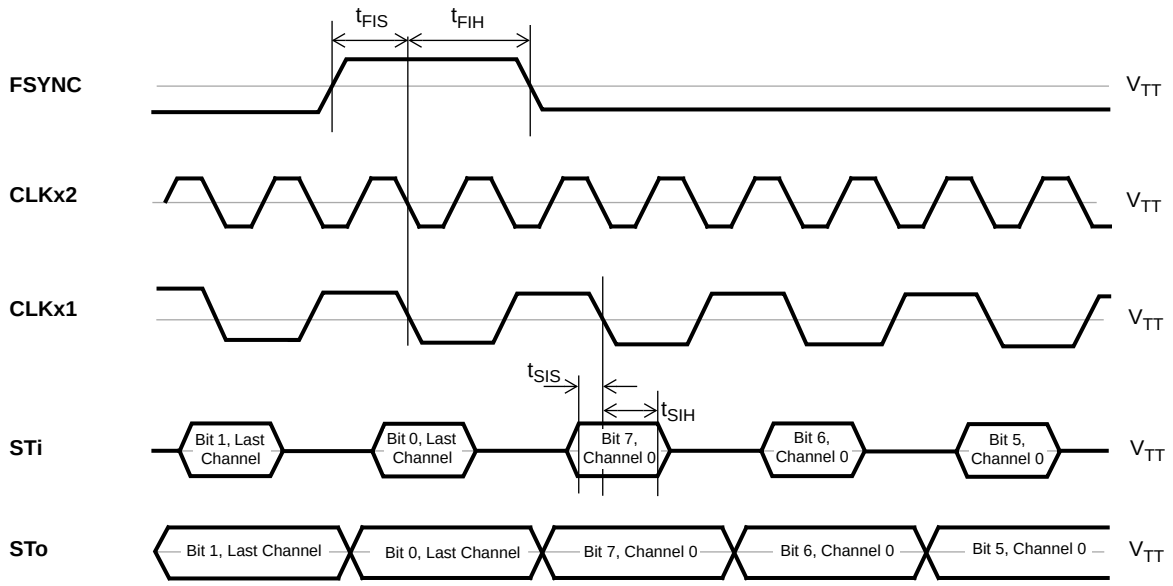


Figure 39 - Main TDM Bus - 2/4 Sampling

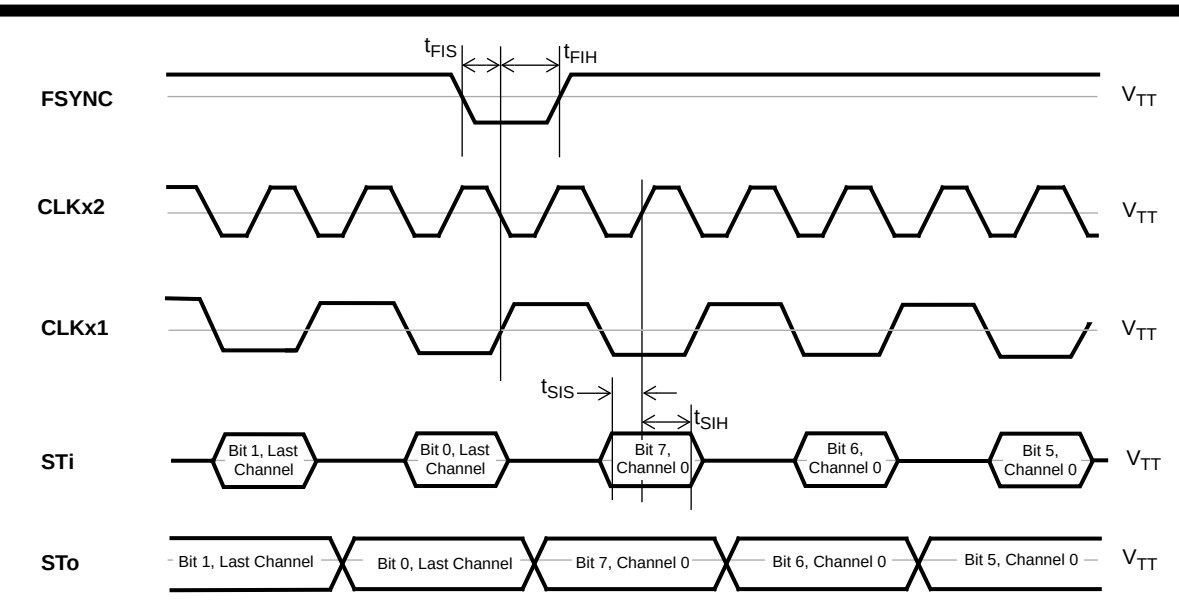


Figure 40 - Main TDM Bus - 3/4 Sampling

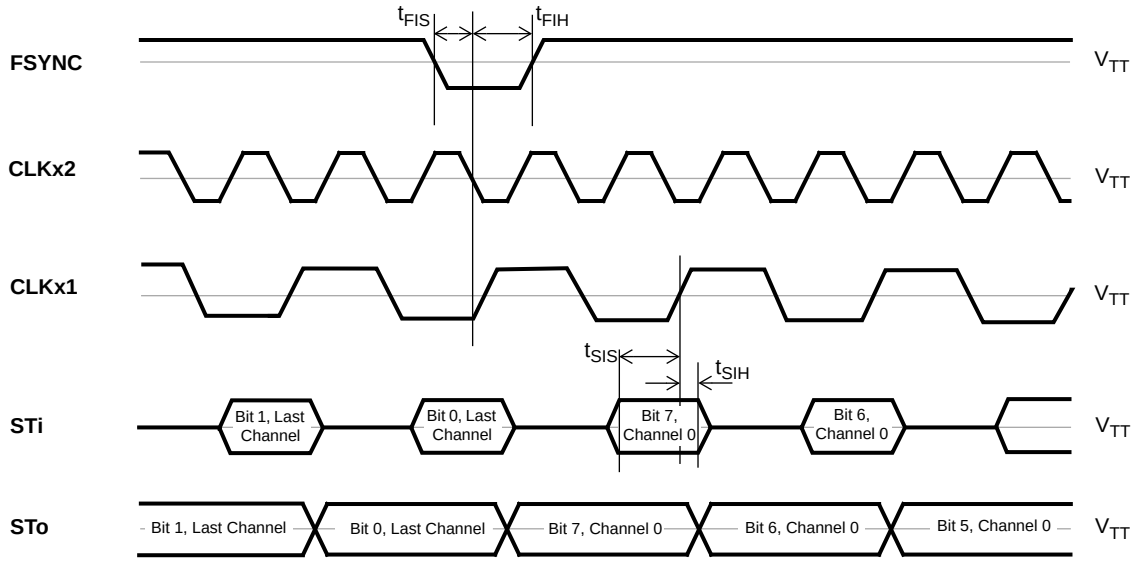


Figure 41 - Main TDM Bus - 4/4 Sampling

6.2.2 Local TDM Bus

Table 77 - Local TDM Bus Clock Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Clock Skew - LOCx2 falling to LOCx1 change	t_{LSK}			10	ns	C_L = 50 pF
LOCx2 Period	t_{Lx2P}		244		ns	
LOCx2 Pulse Width (HIGH / LOW)	$t_{Lx2H/L}$	119	122	125	ns	Input clock = 16.39 MHz (61 ns)
LOCx1 Period	t_{Lx1P}		488		ns	
LOCx1 Pulse Width (HIGH / LOW)	$t_{Lx1H/L}$	241	244	247	ns	
Frame Pulse Width Positive Frame Pulse Negative Frame Pulse	t_{LSW}		 488 244		 ns ns	
Frame Pulse Delay Positive: LOCx2 falling to LSYNC rising Negative: LOCx2 rising to LSYNC falling	t_{LSD}	 0 0		 10 10	 ns ns	C_L = 50 pF
Frame Pulse Guaranteed Setup Positive: LSYNC rising to LOCx2 falling Negative: LSYNC falling to LOCx2 falling	t_{LSS}	 220 98			 ns ns	Input clock = 16.39 MHz (61 ns) C_L = 50 pF
Frame Pulse Guaranteed Hold Positive: LOCx2 falling to LSYNC falling Negative: LOCx2 falling to LSYNC rising	t_{LSH}	 230 108			 ns ns	Input clock = 16.39 MHz (61 ns) C_L = 50 pF
Note: The local bus operates at 2.048 Mbps only.						

Table 78 - Local TDM Bus Data Output Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
LOCSTo Delay - Data to Data Change LOCx1 rising and ((LOCSTo HIGH to LOCSTo LOW) or (LOCSTo LOW to LOCSTo HIGH))	t_{LODX}	5			ns	C_L = 50 pF
LOCSTo Delay - Data to Data Valid LOCx1 rising and ((LOCSTo HIGH to LOCSTo LOW) or (LOCSTo LOW to LOCSTo HIGH))	t_{LODD}			60	ns	C_L = 50 pF
Note 1: The local bus output is never tristated as data is always driven out on LOCSTo. **Note 2:** There is no differentiation between fast bus and slow bus on the local bus.						

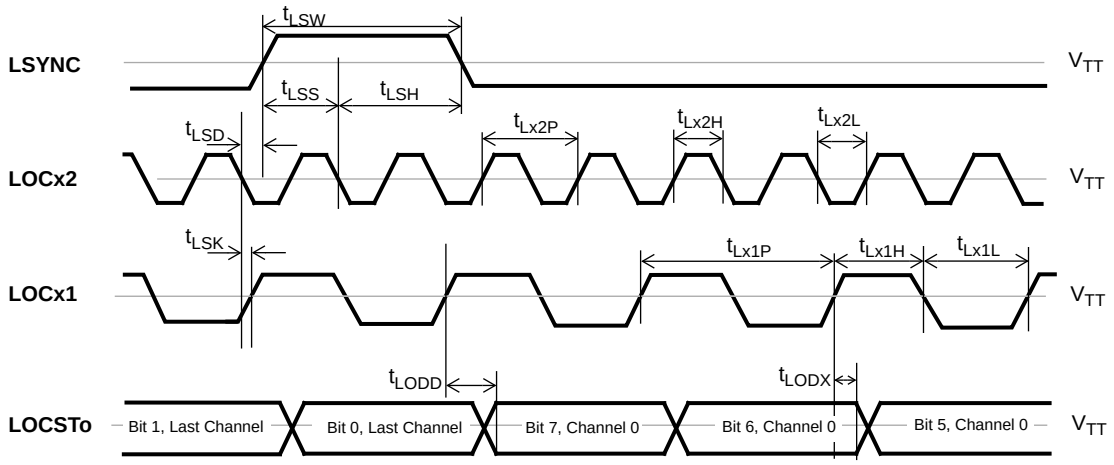


Figure 42 - Local TDM Bus Output Parameters - Positive Frame Pulse

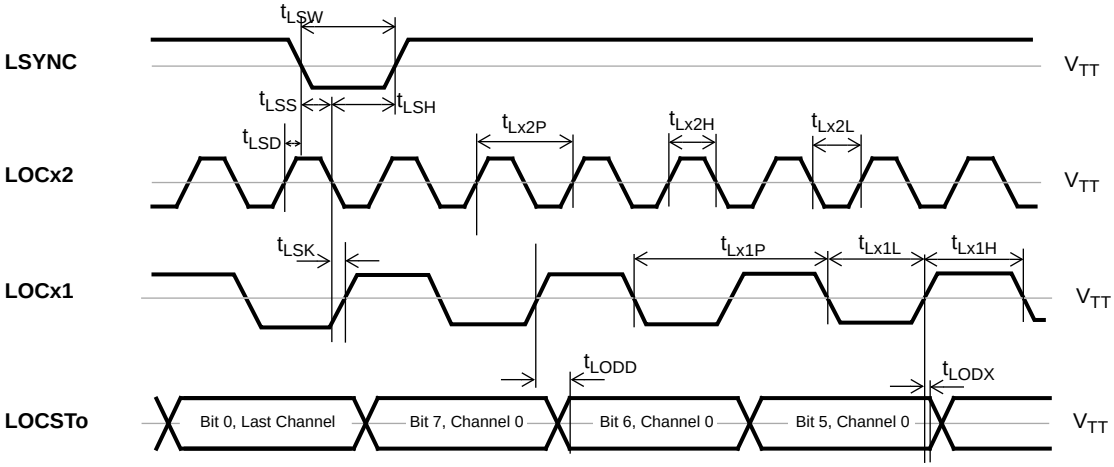


Figure 43 - Local TDM Bus Output Parameters - Negative Frame Pulse

Table 79 - Local TDM Bus Data Input Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
LOCSTi Setup Time - LOCSTi VALID to LOCx1 falling 2/4 Sampling	t_{LIS}	10			ns	
LOCSTi Hold Time - LOCx1 falling to LOCSTi INVALID 2/4 Sampling	t_{LIH}	10			ns	
LOCSTi Setup Time - LOCSTi VALID to LOCx2 rising 3/4 Sampling	t_{LIS}	10			ns	
LOCSTi Hold Time - LOCx2 rising to LOCSTi INVALID 3/4 Sampling	t_{LIH}	5			ns	
LOCSTi Setup Time - LOCSTi VALID to LOCx1 rising 4/4 Sampling	t_{LIS}	10			ns	
LOCSTi Hold Time - LOCx1 rising to LOCSTi INVALID 4/4 Sampling	t_{LIH}	5			ns	

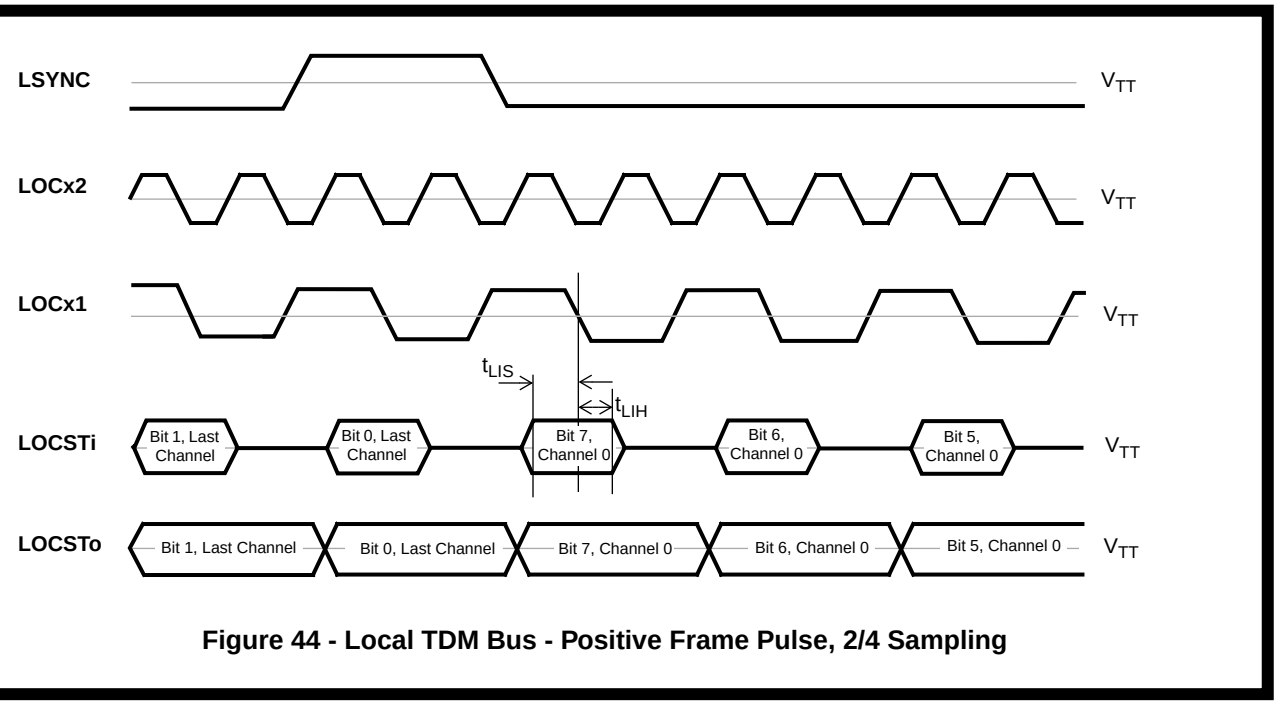


Figure 44 - Local TDM Bus - Positive Frame Pulse, 2/4 Sampling

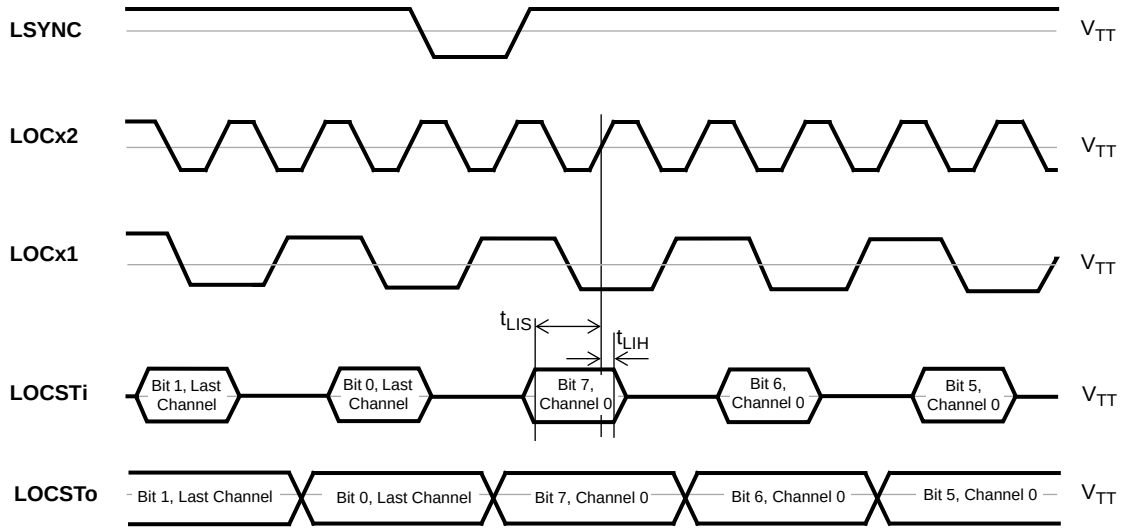


Figure 45 - Local TDM Bus - Negative Frame Pulse, 3/4 Sampling

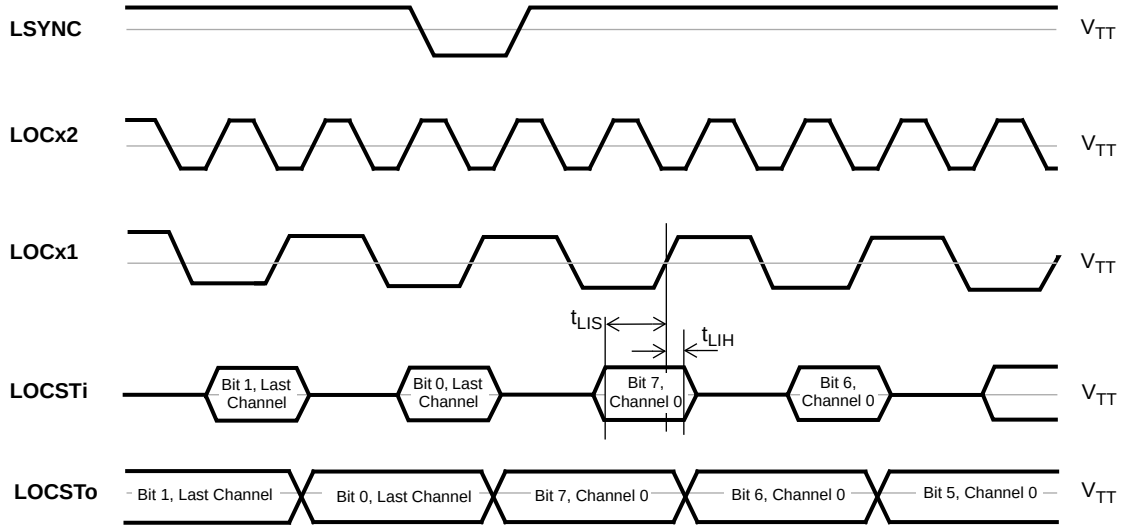


Figure 46 - Local TDM Bus - Negative Frame Pulse, 4/4 Sampling

6.2.3 CPU Interface - Accessing Registers and External Memory

Table 80 - Intel Microprocessor Interface Timing - Read Cycle Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Address Setup - (AEM and A[15:1] VALID) to ($\overline{CS}$ and $\overline{RD}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{RD}$ de-asserted) to (AEM and A[15:1] INVALID)	t_{ADDH}	0			ns	
RDY De-asserted - ($\overline{CS}$ and $\overline{RD}$ asserted) to RDY de-asserted	t_{RDY}			21	ns	1) ~ 1 MCLK cycle + 4 ns 2) C_L = 50 pF
RDY Delay - ($\overline{CS}$ and $\overline{RD}$ asserted) to RDY asserted	t_{RDYD}	100	360	1000	ns	1) 6 MCLK < t_{RDYD} < 60 MCLK 2) C_L = 50 pF
Data Output Setup - D[15:0] VALID to RDY asserted	t_{DS}	15			ns	1) ~ 1 MCLK cycle - 1 ns 2) C_L = 50 pF
Data Output Hold - ($\overline{CS}$ or $\overline{RD}$ de-asserted) to D[15:0] INVALID	t_{DH}	3		15	ns	1) Min. measurement is to D[15:0] INVALID; max. measurement is to D[15:0] high-impedance 2) C_L = 50 pF

Note 1: MCLK = 60 MHz (16.6 ns).
Note 2: Both $\overline{CS}$ and $\overline{RD}$ must be asserted for a read cycle to occur. A read cycle is completed when either $\overline{CS}$ or $\overline{RD}$ is de-asserted.

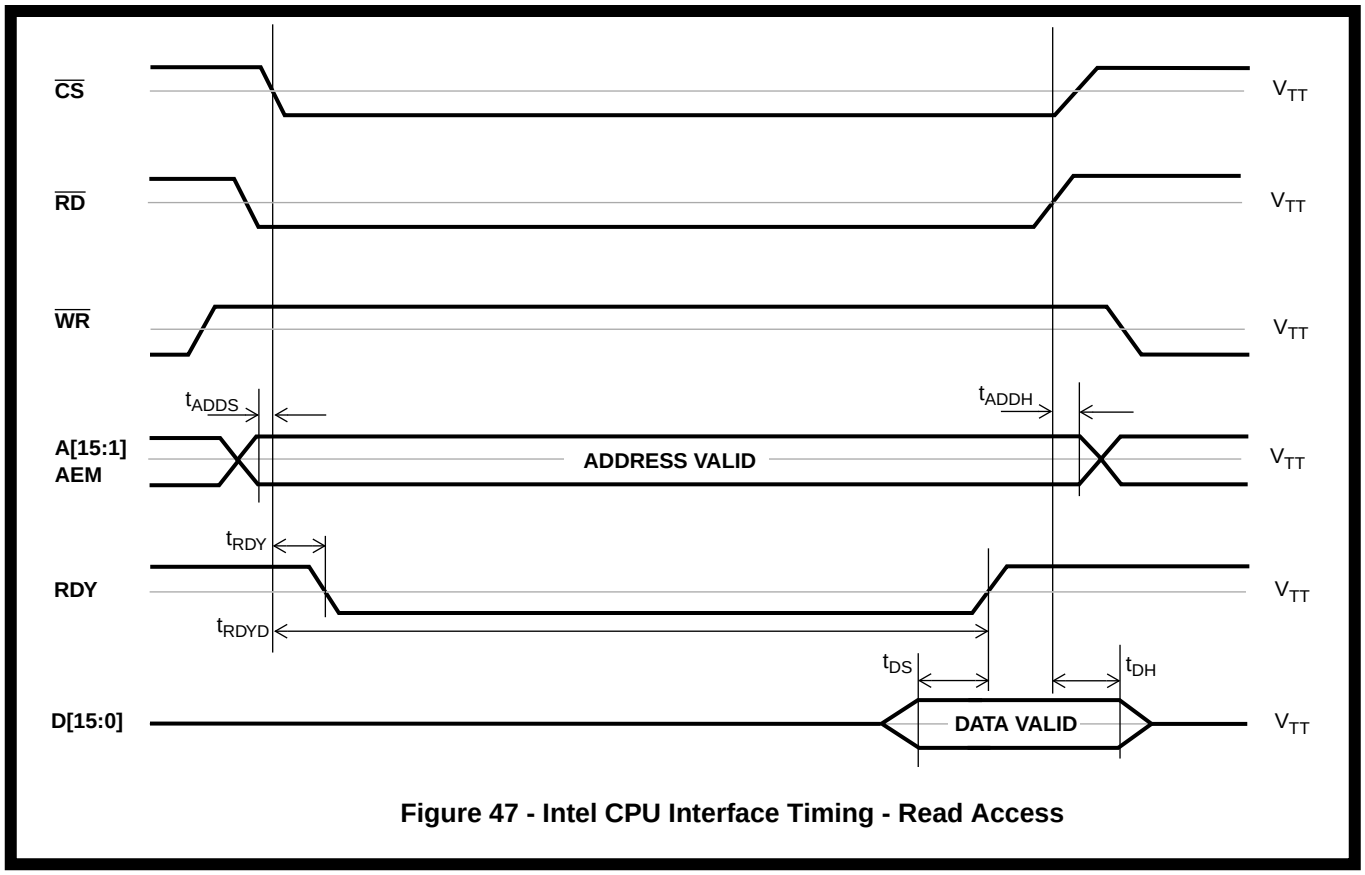


Figure 47 - Intel CPU Interface Timing - Read Access

Table 81 - Intel Microprocessor Interface Timing - Write Cycle Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Address Setup - (AEM and A[15:1] VALID) to ($\overline{CS}$ and $\overline{WR}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{WR}$ de-asserted) to (AEM and A[15:1] INVALID)	t_{ADDH}	0			ns	
RDY De-asserted - ($\overline{CS}$ and $\overline{WR}$ asserted) to RDY de-asserted	t_{RDY}			21	ns	1) ~ 1 MCLK cycle + 4 ns 2) C_L = 50 pF
RDY Delay - ($\overline{CS}$ and $\overline{WR}$ asserted) to RDY asserted	t_{RDYD}	100	415	1000	ns	1) 6 MCLK < t_{RDYD} < 60 MCLK 2) C_L = 50 pF
Write Cycle Hold Time - RDY asserted to ($\overline{CS}$ or $\overline{WR}$ de-asserted)	t_{WRH}	0			ns	
Data Input Setup - D[15:0] VALID to ($\overline{CS}$ and $\overline{WR}$ asserted)	t_{DS}	0			ns	
Data Input Hold - ($\overline{CS}$ or $\overline{WR}$ de-asserted) to D[15:0] INVALID	t_{DH}	0			ns	

Note 1: MCLK = 60 MHz (16.6 ns).
Note 2: Both $\overline{CS}$ and $\overline{WR}$ must be asserted for a write cycle to occur. A write cycle is completed when either $\overline{CS}$ or $\overline{WR}$ is de-asserted.

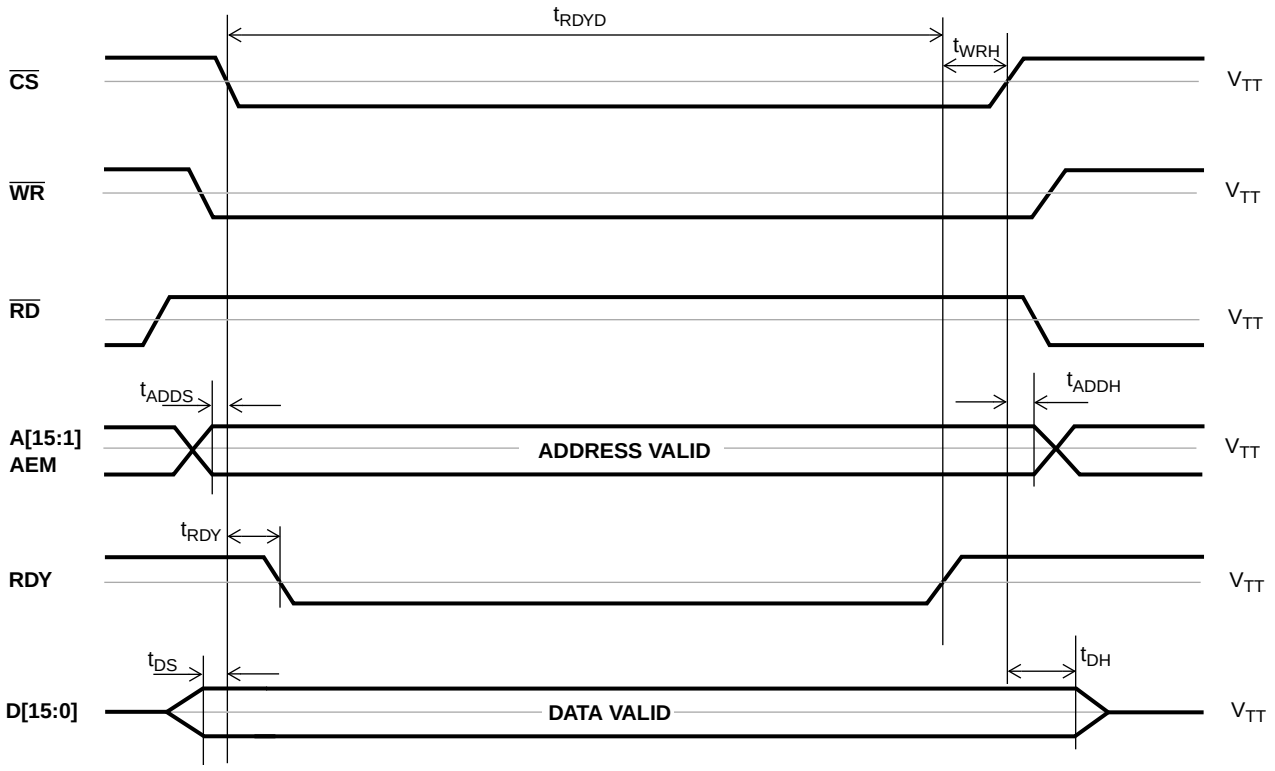


Figure 48 - Intel CPU Interface Timing - Write Access

Table 82 - Motorola Microprocessor Interface Timing - Read Cycle Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Address Setup - (R/$\overline{W}$, AEM and A[15:1] VALID) to ($\overline{CS}$ and $\overline{DS}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to (AEM, A[15:1] and R/$\overline{W}$ INVALID)	t_{ADDH}	0			ns	
$\overline{DTACK}$ High - ($\overline{CS}$ and $\overline{DS}$ asserted) to $\overline{DTACK}$ driving one	t_{DTK1}			34	ns	1) ~ 2 MCLK cycles 2) C_L = 50 pF
$\overline{DTACK}$ Delay - ($\overline{CS}$ and $\overline{DS}$ asserted) to $\overline{DTACK}$ asserted	t_{DTKD}	100	375	1000	ns	1) 6 MCLK < t_{RDYD} < 60 MCLK 2) C_L = 50 pF
Data to $\overline{DTACK}$ Delay - D[15:0] VALID to $\overline{DTACK}$ asserted	t_{DDTK}	14			ns	1) ~ 1 MCLK cycle - 2 ns 2) C_L = 50 pF
$\overline{DTACK}$ Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to $\overline{DTACK}$ driving high	t_{DTKH}	5		15	ns	C_L = 50 pF
$\overline{DTACK}$ High-Impedance - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to $\overline{DTACK}$ high-impedance	t_{DTKZ}	6		20	ns	C_L = 50 pF
Data Output Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to D[15:0] INVALID	t_{DH}	3		15	ns	1) Min. measurement is to D[15:0] INVALID; max. measurement is to D[15:0] high-impedance 2) C_L = 50 pF

Note 1: MCLK = 60 MHz (16.6 ns).
Note 2: Both $\overline{CS}$ and $\overline{DS}$ must be asserted for a read cycle to occur. A read cycle is completed when either $\overline{CS}$ or $\overline{DS}$ is de-asserted.

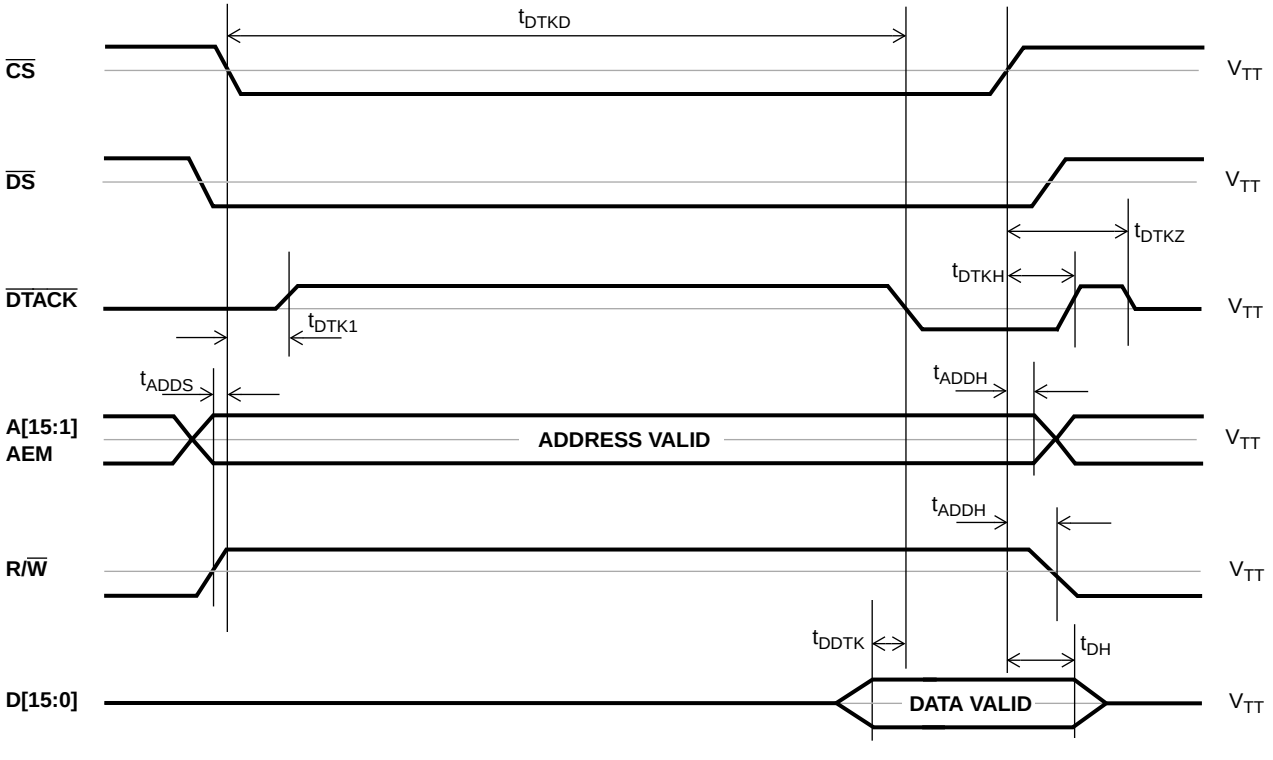


Figure 49 - Motorola CPU Interface Timing - Read Access

Table 83 - Motorola Microprocessor Interface Timing - Write Cycle Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Address Setup - (R/$\overline{W}$, AEM and A[15:1] VALID) to ($\overline{CS}$ and $\overline{DS}$ asserted)	t_{ADDS}	0			ns	
Address Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to (AEM, A[15:1] and R/$\overline{W}$ INVALID)	t_{ADDH}	0			ns	
$\overline{DTACK}$ High - ($\overline{CS}$ and $\overline{DS}$ asserted) to $\overline{DTACK}$ driving one	t_{DTK1}			34	ns	1) ~ 2 MCLK cycles 2) C_L = 50 pF
$\overline{DTACK}$ Delay - ($\overline{CS}$ and $\overline{DS}$ asserted) to $\overline{DTACK}$ asserted	t_{DTKD}	100	420	1000	ns	1) 6 MCLK < t_{RDYD} < 60 MCLK 2) C_L = 50 pF
$\overline{DTACK}$ Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to $\overline{DTACK}$ driving high	t_{DTKH}	5		15	ns	C_L = 50 pF
$\overline{DTACK}$ High-Impedance - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to $\overline{DTACK}$ high-impedance	t_{DTKZ}	6		20	ns	C_L = 50 pF
Data Input Setup - D[15:0] VALID to ($\overline{CS}$ and $\overline{DS}$ asserted)	t_{DS}	0			ns	C_L = 50 pF
Data Input Hold - ($\overline{CS}$ or $\overline{DS}$ de-asserted) to D[15:0] INVALID	t_{DH}	0			ns	C_L = 50 pF

Note 1: MCLK = 60 MHz (16.6 ns).
Note 2: Both $\overline{CS}$ and $\overline{DS}$ must be asserted for a write cycle to occur. A write cycle is completed when either $\overline{CS}$ or $\overline{DS}$ is de-asserted.

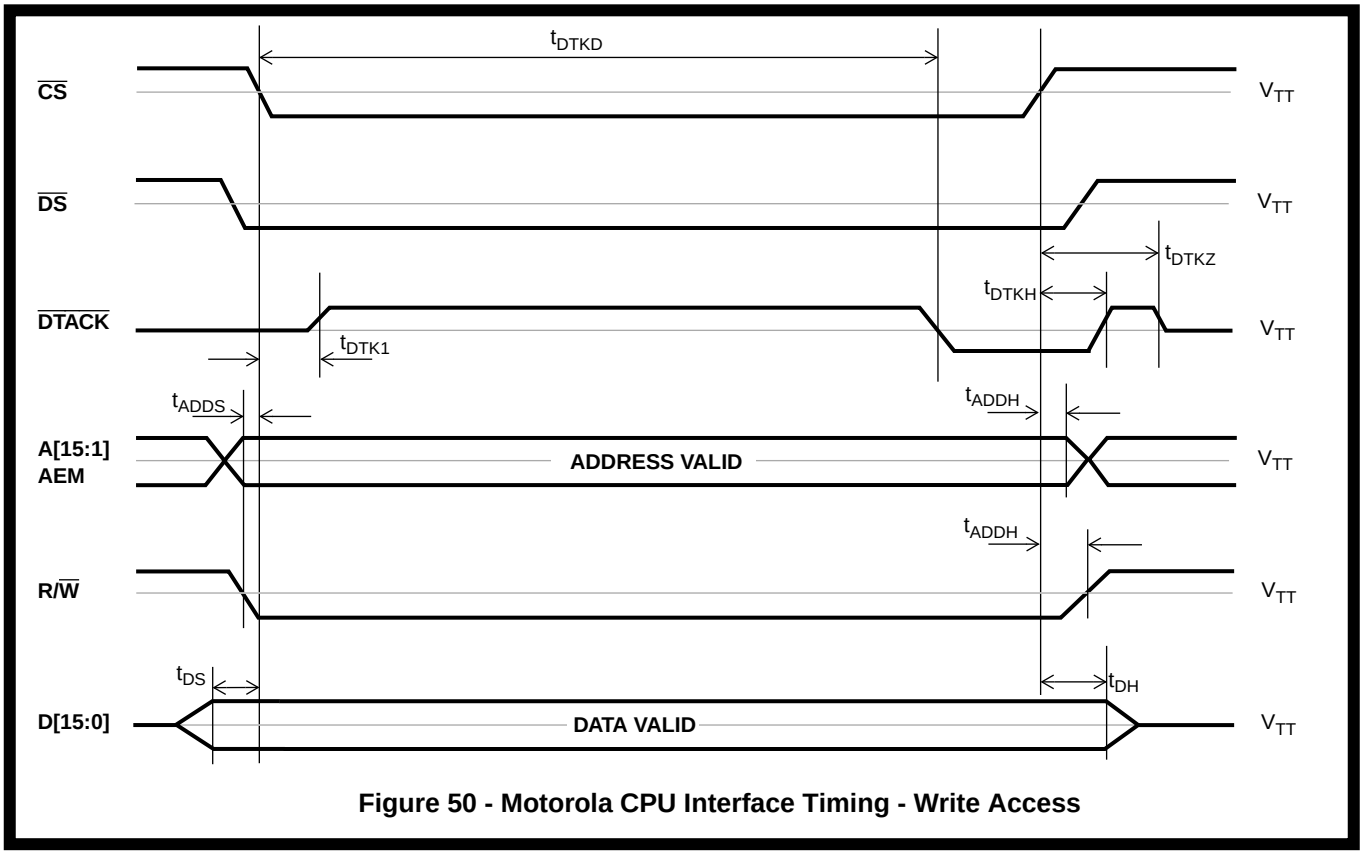


Figure 50 - Motorola CPU Interface Timing - Write Access

6.2.4 Interface with External Memory

Table 84 - MCLK - Master Clock Input Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
MCLK Frequency	t_{MF}		60	60.006	MHz	
MCLK Period	t_{MP}		16.7		ns	
MCLK Pulse Width (HIGH / LOW)	$t_{MH/L}$	7.5	8.33		ns	

Table 85 - External Memory Interface Timing - Clock Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
MEMCLK Period	t_{MEMP}		16.7		ns	MEMCLK = MCLK = 60 MHz
MEMCLK Pulse Width (HIGH / LOW)	$t_{MEMH/L}$	7.6	8.33	9.1	ns	MCLK = 16.7 ns period, 50/50 duty cycle
		6.7	8.33	10.0	ns	MCLK = 16.7 ns period, 45/55 duty cycle

Table 86 - External Memory Interface Timing - Read Cycle Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Data Input Setup - (MEM_DAT[31:0] and MEM_PAR[3:0] VALID) to MEMCLK rising	t_{DIS}	5			ns	
Data Input Hold Time - MEMCLK rising to (MEM_DAT[31:0] and MEM_PAR[3:0] INVALID)	t_{DIH}	1			ns	
Output Delay - MEMCLK rising to (MEM_ADD[17:0] VALID and $\overline{\text{MEM\_CS[1:0][H/L]}}$ and $\overline{\text{MEM\_WR[3:0]}}$ asserted)	t_{OD}			10	ns	C_L = 50 pF
Output Hold Time - MEMCLK rising to (MEM_ADD[17:0] INVALID and $\overline{\text{MEM\_CS[1:0][H/L]}}$ and $\overline{\text{MEM\_WR[3:0]}}$ de-asserted)	t_{OH}	1.5			ns	C_L = 50 pF
Note: $\overline{\text{MEM\_OE}}$ is continuously asserted low after reset.						

Table 87 - External Memory Interface Timing - Write Cycle Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
Output Delay - MEMCLK rising to (MEM_ADD[17:0], MEM_DAT[31:0] and MEM_PAR[3:0] VALID) and ($\overline{\text{MEM\_CS[1:0][H/L]}}$ and $\overline{\text{MEM\_WR[3:0]}}$ asserted)	t_{OD}			11	ns	C_L = 50 pF
Output Hold Time - MEMCLK rising to (MEM_ADD[17:0], MEM_DAT[31:0] and MEM_PAR[3:0] INVALID) and ($\overline{\text{MEM\_CS[1:0][H/L]}}$ and $\overline{\text{MEM\_WR[3:0]}}$ de-asserted)	t_{OH}	1.5			ns	C_L = 50 pF
High-Z to Drive Time - MEMCLK rising to (MEM_DAT[31:0] and MEM_PAR[3:0] change)	t_{ZD}	1			ns	C_L = 50 pF Minimum hold in High-Z
Note: $\overline{\text{MEM\_OE}}$ is continuously asserted low after reset.						

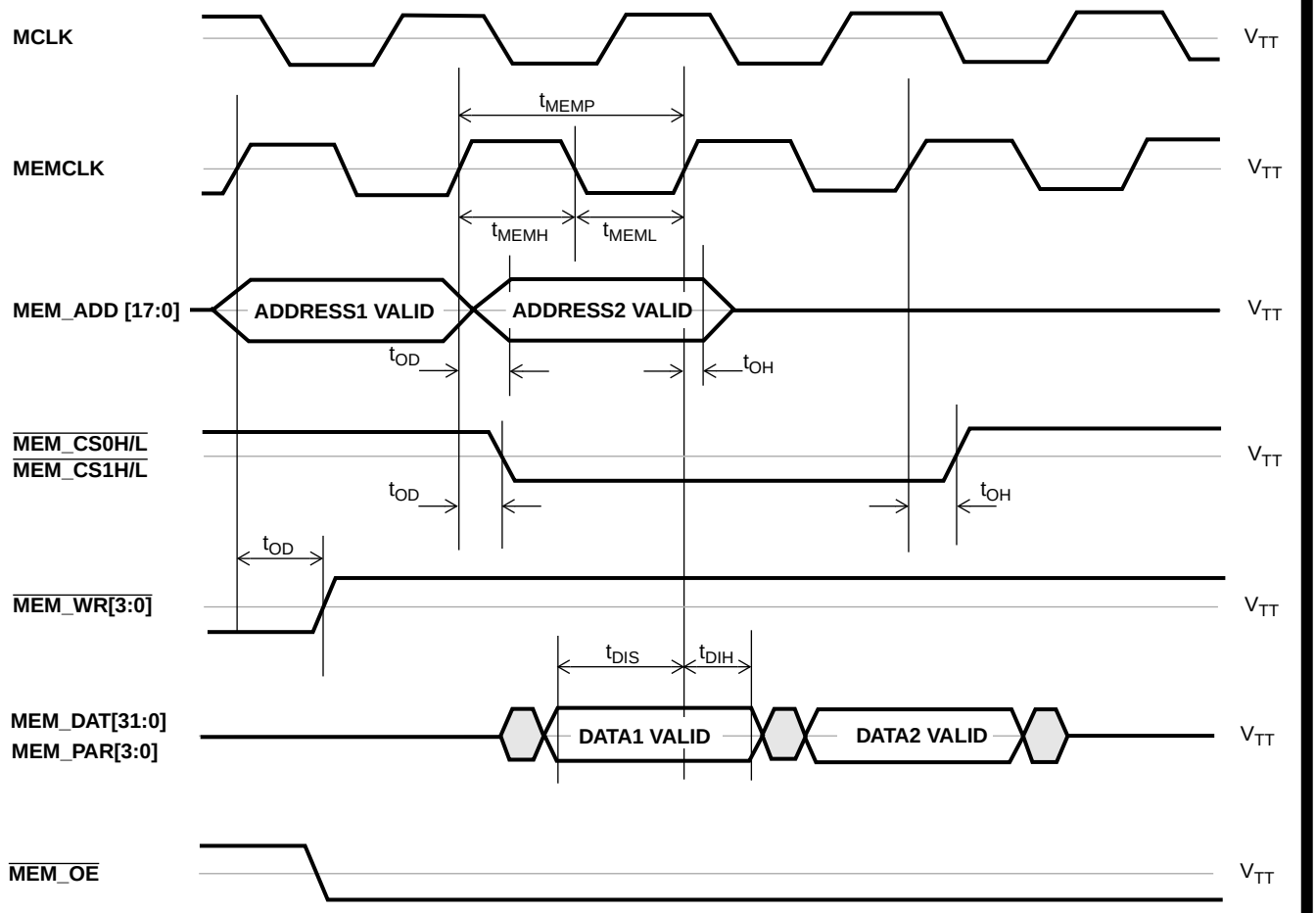


Figure 51 - External Memory Interface Timing - Read Cycle

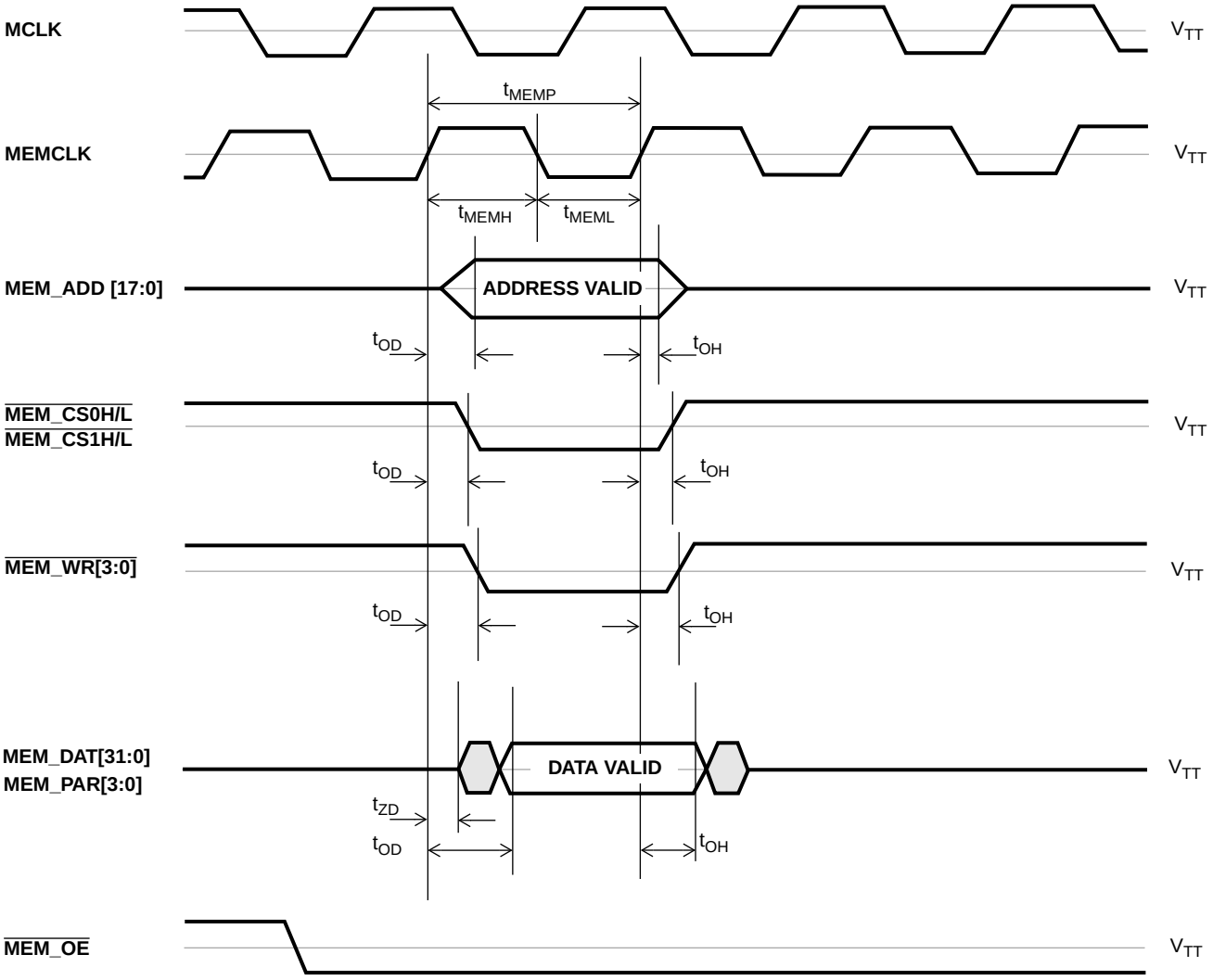


Figure 52 - External Memory Interface Timing - Write Cycle

6.2.5 UTOPIA Interfaces

6.2.5.1 Primary UTOPIA Interface

Table 88 - Primary UTOPIA Interface Timing - Transmit

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
PTXCLK Period	t_{PTXP}		40		ns	PTXCLK = 25 MHz
PTXCLK Pulse Width (HIGH / LOW)	$t_{PTXH/L}$	16	20	24	ns	
Input Setup Time - PTXCLAV VALID to PTXCLK rising	t_{PTXIS}	10			ns	
Input Hold Time - PTXCLK rising to PTXCLAV de-asserted	t_{PTXIH}	1			ns	
Output Delay - PTXCLK rising to (PTXDATA[7:0] VALID and $\overline{\text{PTXEN}}$ and PTXSOC asserted)	t_{PTXD}			20	ns	C_L = 50 pF
Output Hold Time - PTXCLK rising to (PTXDATA[7:0] INVALID and $\overline{\text{PTXEN}}$ and PTXSOC de-asserted)	t_{PTXH}	1			ns	C_L = 50 pF
Note: The MT90500 operates with the UTOPIA cell-level handshake.						

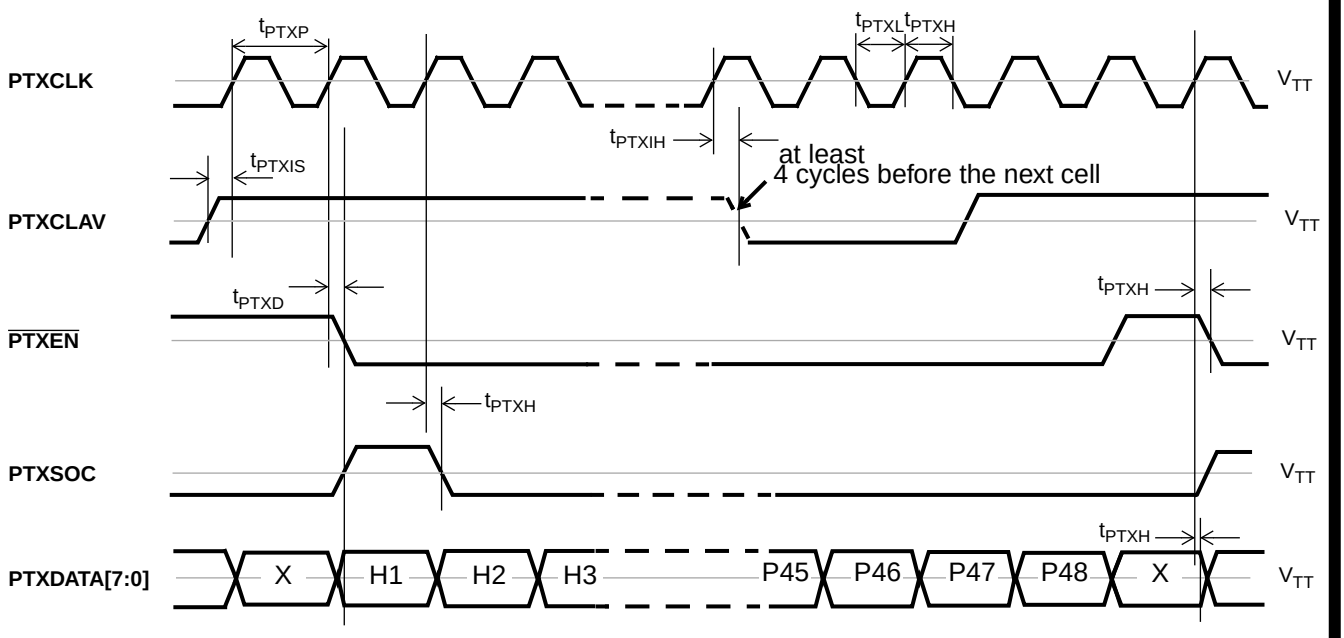


Figure 53 - Primary UTOPIA Bus - Transmit Timing

Table 89 - Primary UTOPIA Interface Timing - Receive

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
PRXCLK Period	t_{PRXP}		40		ns	PRXCLK = 25 MHz
PRXCLK Pulse Width (HIGH / LOW)	$t_{PRXH/L}$	16	20	24	ns	
Input Setup Time - (PRXCLAV, $\overline{\text{PRXEN}}$, PRXSOC asserted and PRXDATA[7:0] VALID) to PRXCLK rising	t_{PRXIS}	10			ns	
Input Hold Time - PRXCLK rising to (PRXDATA[7:0] INVALID and PRXSOC, PRXCLAV, and $\overline{\text{PRXEN}}$ de-asserted)	t_{PRXIH}	1			ns	

Note: The MT90500 operates with the UTOPIA cell-level handshake.

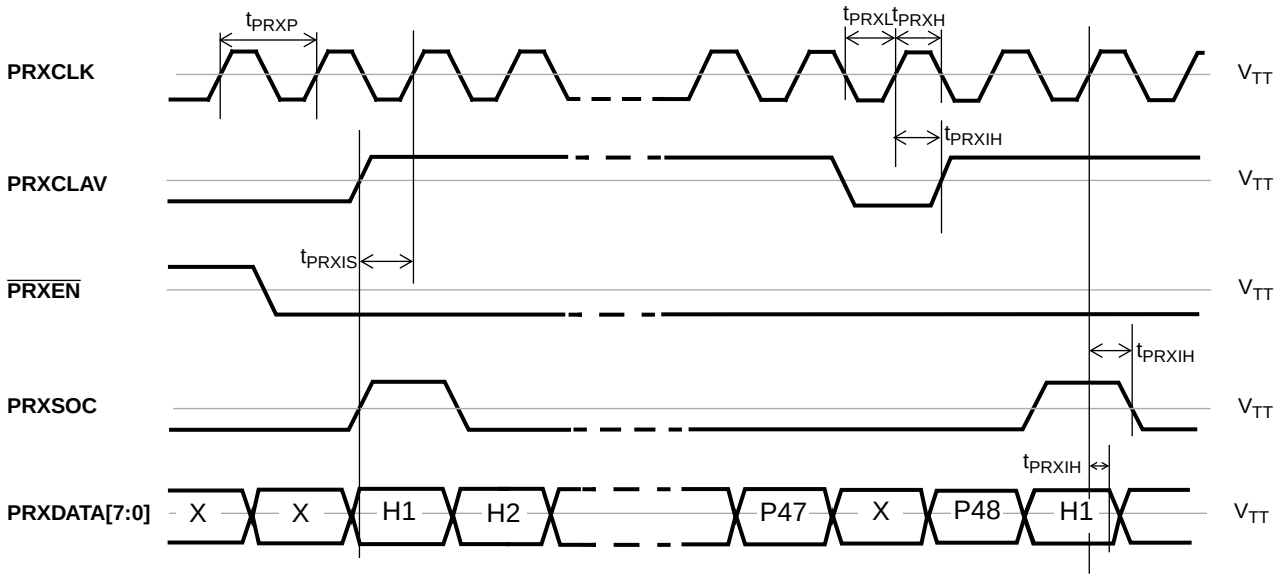


Figure 54 - Primary UTOPIA Bus - Receive Timing

6.2.5.2 Secondary UTOPIA Interface

Table 90 - Secondary UTOPIA Interface Timing

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
STXCLK Period	t_{STXP}		40		ns	STXCLK = 25 MHz
STXCLK Pulse Width (HIGH / LOW)	$t_{STXH/L}$	16	20	24	ns	
Input Setup Time - (STXDATA[7:0] VALID; STXSOC and $\overline{STXEN}$ asserted) to STXCLK rising	t_{STXIS}	10			ns	
Input Hold Time - STXCLK rising to (STXDATA[7:0] INVALID and STXSOC and $\overline{STXEN}$ de-asserted)	t_{STXIH}	1			ns	
Output Delay - STXCLK rising to STXCLAV asserted	t_{STXD}			20	ns	C_L = 50 pF
Output Hold Time - STXCLK rising to STXCLAV de-asserted	t_{STXH}	1				C_L = 50 pF

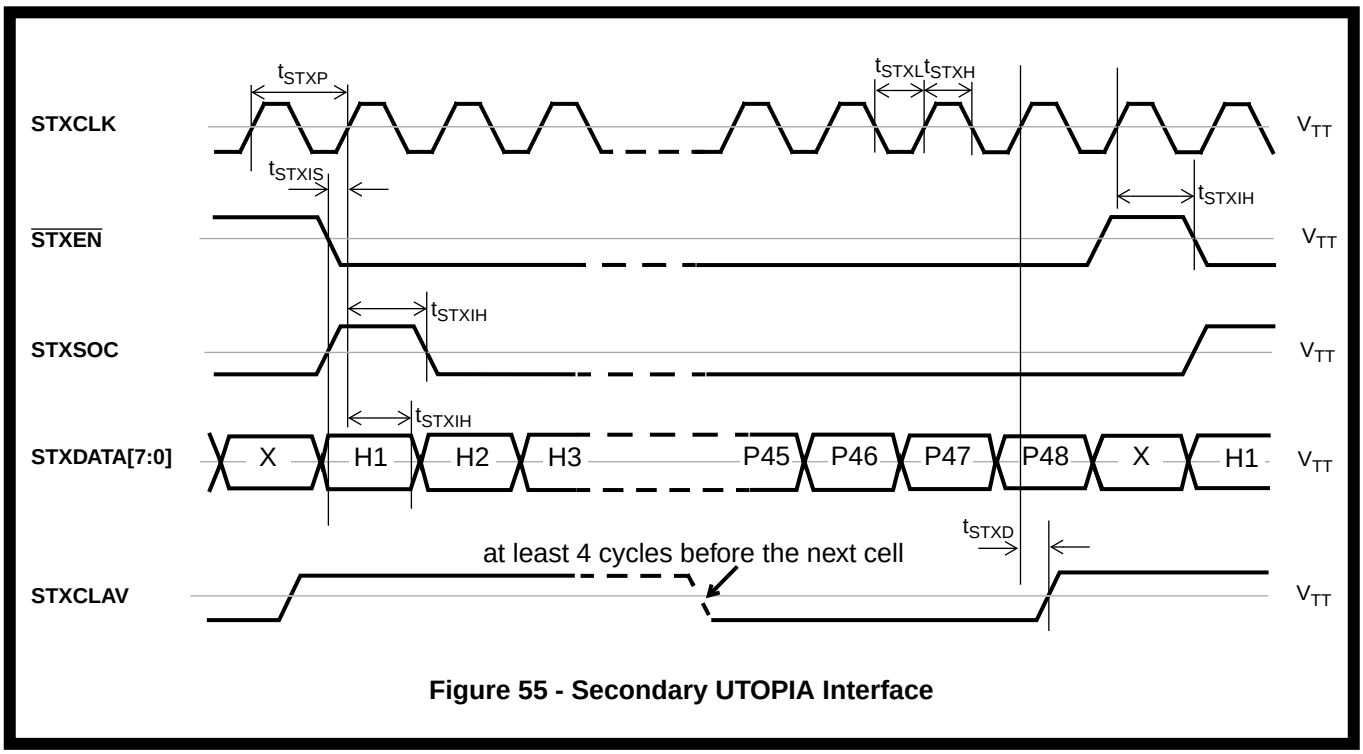


Figure 55 - Secondary UTOPIA Interface

6.2.6 Message Channel Interface

Table 91 - Message Channel Clock Parameters

Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
MCCLK Period	t_{MCCP}		488		ns	
MCCLK Pulse Width (HIGH / LOW)	$t_{MCCH/L}$	237	244	252	ns	CLKX2 period 244 ns, 122 ns or 61 ns.
Skew - CLKx2 falling to MCCLK change	t_{MCCD}	5		22	ns	C_L = 50 pF
Transmit Delay - MCTX to MC MCTX falling to MC falling MCTX rising to MC High-Z	 t_{MCTDL} t_{MCTDZ}	 4 3		 16 13	ns	C_L = 50 pF
Receive Delay - MC to MCRX MC falling to MCRX falling MC rising to MCRX rising	t_{MCRD}	 4 3		 15 14	ns	C_L = 50 pF

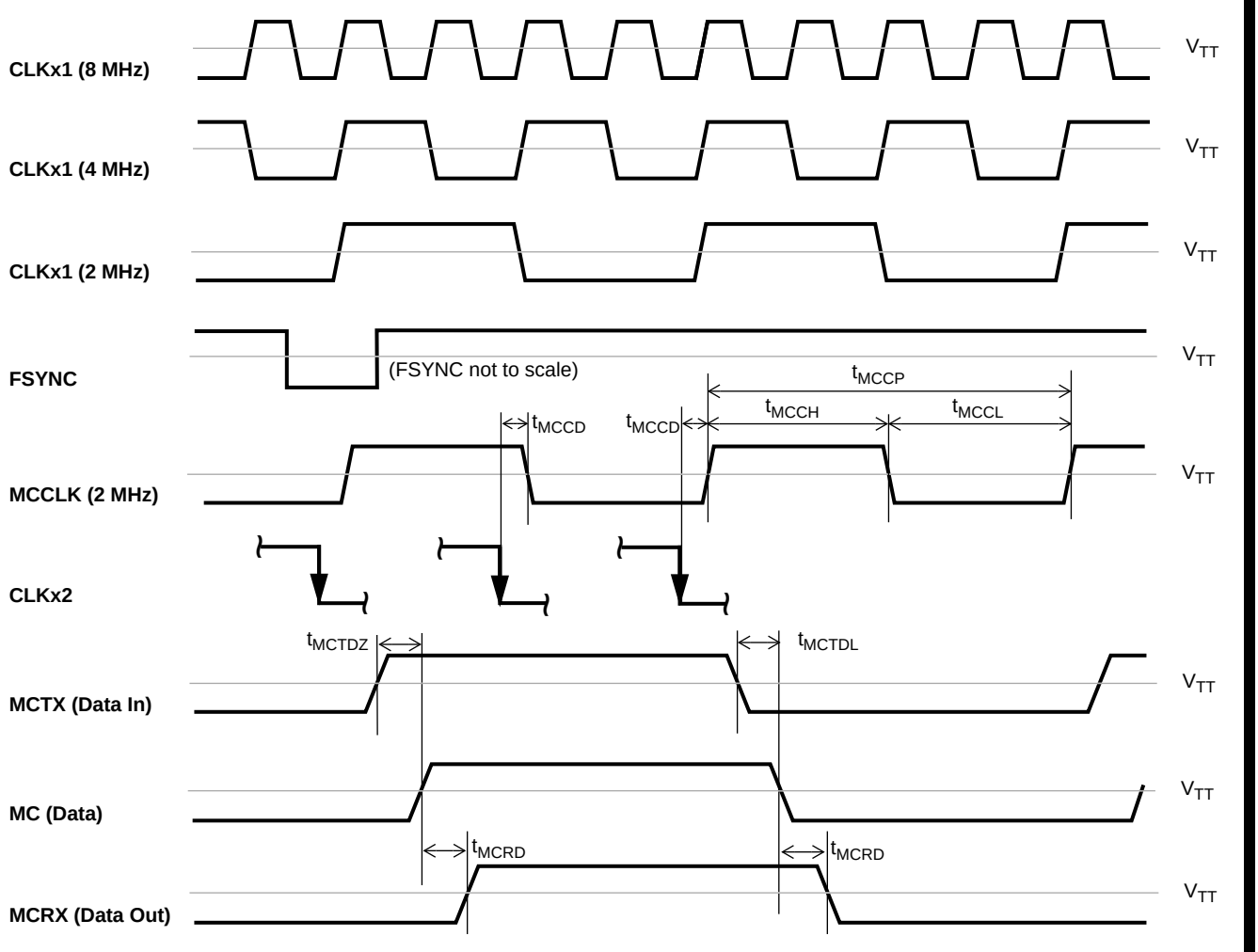


Figure 56 - Message Channel Timing

7. Applications

7.1 Board Level Applications

Figure 57 shows a general board level application for the MT90500. This shows a high-level view of the device connection to external memory, a CPU, an ATM Physical Layer device, an ATM AAL5 SAR device, and the TDM backplane.This is a general application diagram; the most frequent variations would be: the number and size of the SSRAM chips, the type of CPU or PHY, the mode of the TDM backplane and TDM local bus (several possibilities are listed in the figure), and the presence or absence of a secondary SAR.

The size of external memory is selected to suit the application, and is tied to the number of TDM 64 kbps channels to be used, the number of VCs to be used, and the Cell Delay Variation tolerance of the receive channels. Similarly the CPU and PHY are chosen to suit the application. The TDM backplane mode (positive or negative frame-pulse; fast or slow hold time; and 2.048, 4.096, or 8.192 Mbps) is application selectable, and the local TDM bus can be enabled for applications which require it (e.g. when it is desirable to have a local HDLC, or DSP, which is not tied to the backplane). The secondary SAR may be used in applications which require ATM signalling, though it is possible to do a moderate amount of signalling using the TX and RX Data FIFOs in the MT90500, provided that the CPU can perform the rest of the SAR functions in software.

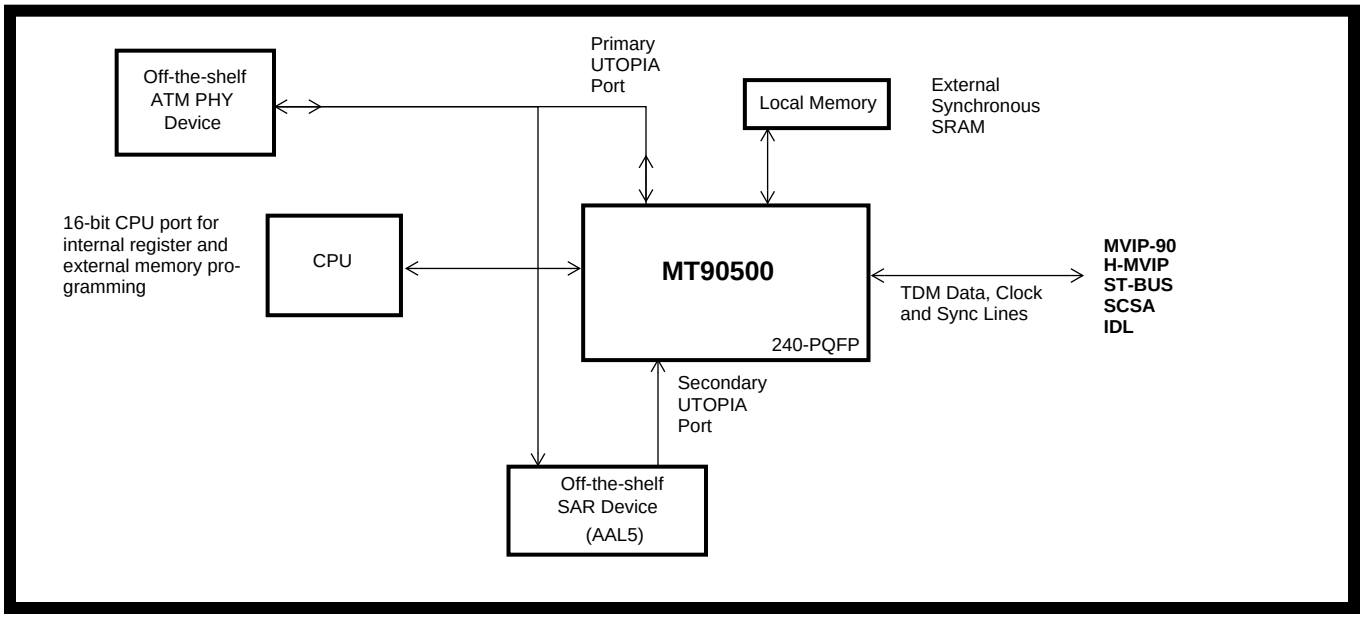


Figure 57 - MT90500 Device Application Block Diagram

The MT90500 will work with a variety of standard Synchronous SRAM parts. The burst feature of the Synchronous SRAM is not used by the MT90500, and since the SSRAM is not connected to a cache controller, some of the control pins of most SSRAMS are not used by the MT90500. The common control pin names for the SSRAM, and their connections when used with the MT90500, are listed in Table 92, and Table 93.

The Secondary UTOPIA bus of the MT90500, and the Transmit UTOPIA multiplexer, allow application flexibility in working with a variety of off-the-shelf data SARs. This feature also allows two MT90500s to be combined for a full 2048 full-duplex TDM channel application (allowing full connection to a 4096 channel backplane). Note that each MT90500 carries 1024 channels in each direction, not 2048 transmitted by one MT90500, and 2048 received by the other MT90500. The capabilities of the TX SAR and RX SAR internal blocks are balanced at 1024 channels.

Figure 58 shows in greater detail an example of the UTOPIA bus connections when two MT90500 devices and a secondary AAL5 SAR are used. Note that the receive UTOPIA bus is controlled by $\overline{\text{RXEN}}$ of the secondary AAL5 SAR. If the secondary SAR is too slow, or configured badly, it will throttle-back the cells output by the PHY device, and cause lost cells or increased CDV. ($\overline{\text{RXEN}}$ may also be tied low to allow full speed cell reception.) The MT90500 allows the primary UTOPIA port transmit clock (PTXCLK) to be one of: the transmit clock of the secondary SAR (STXCLK), the master clock (MCLK) divided by 2 or 4, or an external source. The

Table 92 - MT90500 Connections to 18-bit Synchronous SRAM

Pin Function	SSRAM	MT90500	Notes
Address	A0-A14	MEM_ADD[14:0]	
Data	DQ[0:7, 9:16]	MEM_DAT[15:0], or MEM_DAT[31:16]	MEM_DAT[31:16] used for second SSRAM chip.
Underrun Flag	DQ[8, 17]	MEM_PAR[1:0], or MEM_PAR[3:2]	MEM_PAR[3:2] used for second SSRAM chip.
Lower Byte Write Enable	LW*	$\overline{\text{MEM\_WR[0]}}$, or $\overline{\text{MEM\_WR[2]}}$	$\overline{\text{MEM\_WR[2]}}$ used for second SSRAM chip.
Upper Byte Write Enable	UW*	$\overline{\text{MEM\_WR[1]}}$, or $\overline{\text{MEM\_WR[3]}}$	$\overline{\text{MEM\_WR[3]}}$ used for second SSRAM chip.
Memory Clock	K	MEMCLK	
Chip Enable	E*	$\overline{\text{MEM\_CS0L}}$, or $\overline{\text{MEM\_CS0H}}$, or $\overline{\text{MEM\_CS1L}}$, or $\overline{\text{MEM\_CS1H}}$	$\overline{\text{MEM\_CS0H}}$ used for second SSRAM chip. $\overline{\text{MEM\_CS1x}}$ used for second bank of SSRAM chips.
Output Enable	G*	$\overline{\text{MEM\_OE}}$	
Burst Address Advance	ADV*	-	Never enabled - pull to VDD to disable
Processor Address Status	ADSP*	-	Never enabled - pull to VDD to disable
Controller Address Status	ADSC*	-	Always enabled - tie to GND to enable

Note: The pin names in this table correspond to those for the Motorola 32K x 18-bit BurstRAM Synchronous Fast Static RAM (MCM67H518).

Table 93 - MT90500 Connections to 32/36-bit Synchronous SRAM

Pin Function	MCM69F536A	CY7C1329	MT90500	Notes
Address	SA	A	MEM_ADD]	
Data	DQ	DQ[31:0]	MEM_DAT[31:0]	
Underrun Flag	DQ8[d:a]	(pull-up)	MEM_PAR[3:0]	If TDM Underrun Error indication not used, pull-up MEM_PAR[3:0] to V_{DD3}.
Byte Write	SB*[d:a]	BW*[3:0]	$\overline{\text{MEM\_WR[3:0]}}$	
Global Write	SGW*	GW*	-	Tie high (disable global writes)
Byte Write Enable	SW*	BWE*	-	Tie low (enable byte-writes)
Clock	K	CLK	MEMCLK	
Chip Enable 1	SE1*	CE1*	-	Tie low (enable)
Chip Enable 2	SE2	CE2	-	Tie high (enable)
Chip Enable 3	SE3*	CE3*	$\overline{\text{MEM\_CS0L}}$	$\overline{\text{MEM\_CS1L}}$ used for second bank/ chip.
Output Enable	G*	OE*	$\overline{\text{MEM\_OE}}$	
Burst Address Advance	ADV*	ADV*	-	Tie high (disable)
Processor Address Status	ADSP*	ADSP*	-	Tie high (disable)
Controller Address Status	ADSC*	ADSC*	-	Tie low (enable)
Sleep	-	ZZ	-	Tie low
Burst Mode	LBO*	MODE	-	Tie low or tie high
no connect	-	-	$\overline{\text{MEM\_CSxH}}$	$\overline{\text{MEM\_CSxH}}$ not used with 32/36 bit memory

primary UTOPIA port receive clock (PRXCLK) is driven by the secondary SAR, or it is tied to PTXCLK if a secondary SAR is not present. PRXCLK should not be too slow, or CDV may be increased.

7.2 System Level Applications

Figure 59 depicts an ATM adapter card within a work-group hub, switching non-CBR data and CBR voice traffic with 2 internal switching backplanes (a TDM and a packet bus). The MT90500 device interfaces to the bus transporting CBR traffic such as voice or video conferencing and the external AAL5 SAR device interfaces to either a management bus or user data bus such as PCI. Figure 60 shows a block diagram of the card.

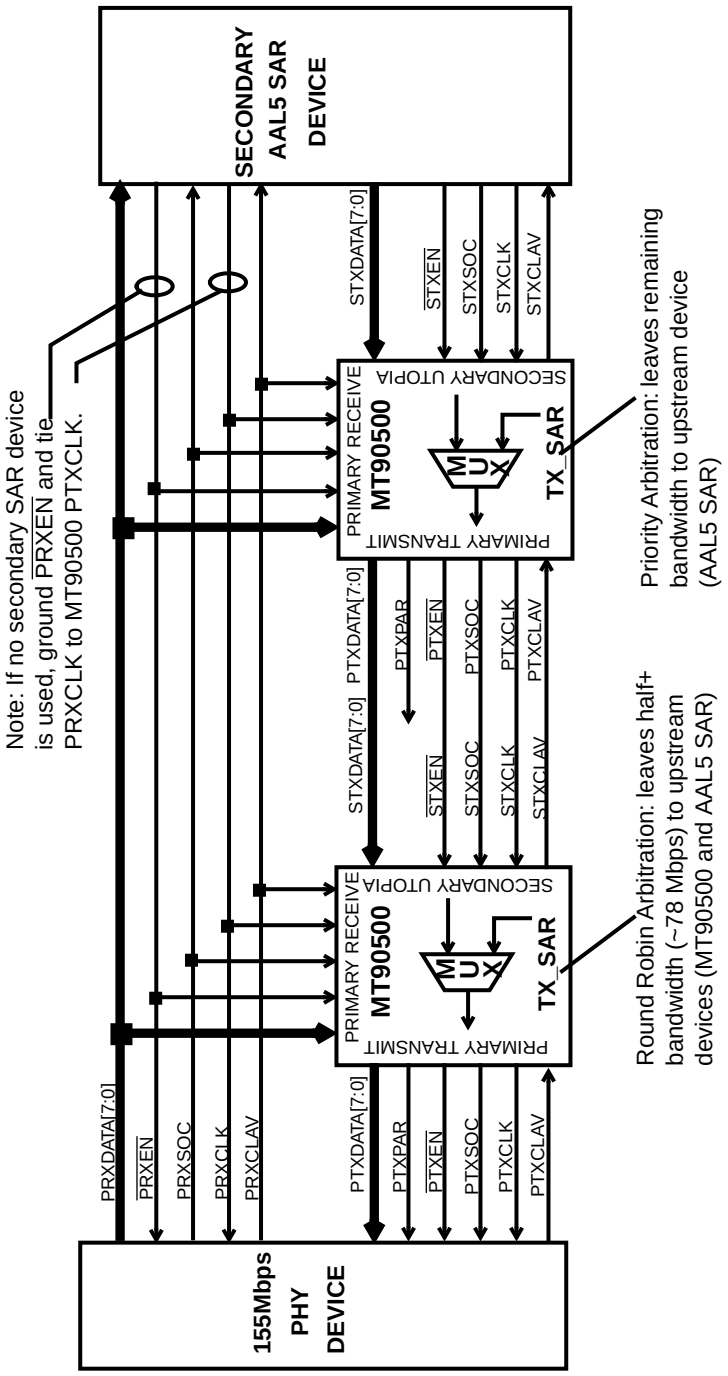


Figure 58 - UTOPIA Bus Interconnections for Two MT90500s and an AAL5 SAR

Figure 61 shows a networking product such as an access concentrator using the MT90500 to perform conversion from TDM links coming out of T1/E1 trunks and the user's internal ATM backplane. An external converter might be used to change the MT90500's UTOPIA interface to the user's ATM bus.

Figure 62 shows an application where TDM traffic must be transported across a proprietary cell bus. The interface chips transform the standard UTOPIA format cells of the MT90500 into the proprietary cell format.

Figure 63 and Figure 64 show how the MT90500 device can be used within a Computer Telephony Integration (CTI) system to transport CBR traffic from multi-stream MVIP or SCSA buses across an ATM link.

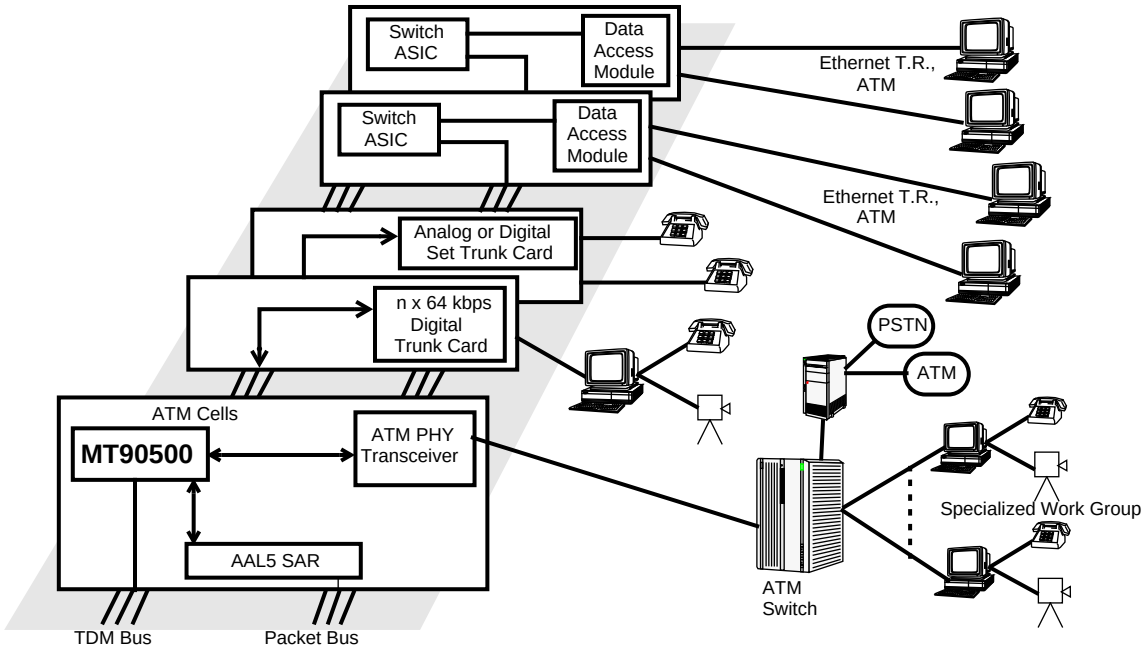


Figure 59 - The MT90500 within a LAN Hub

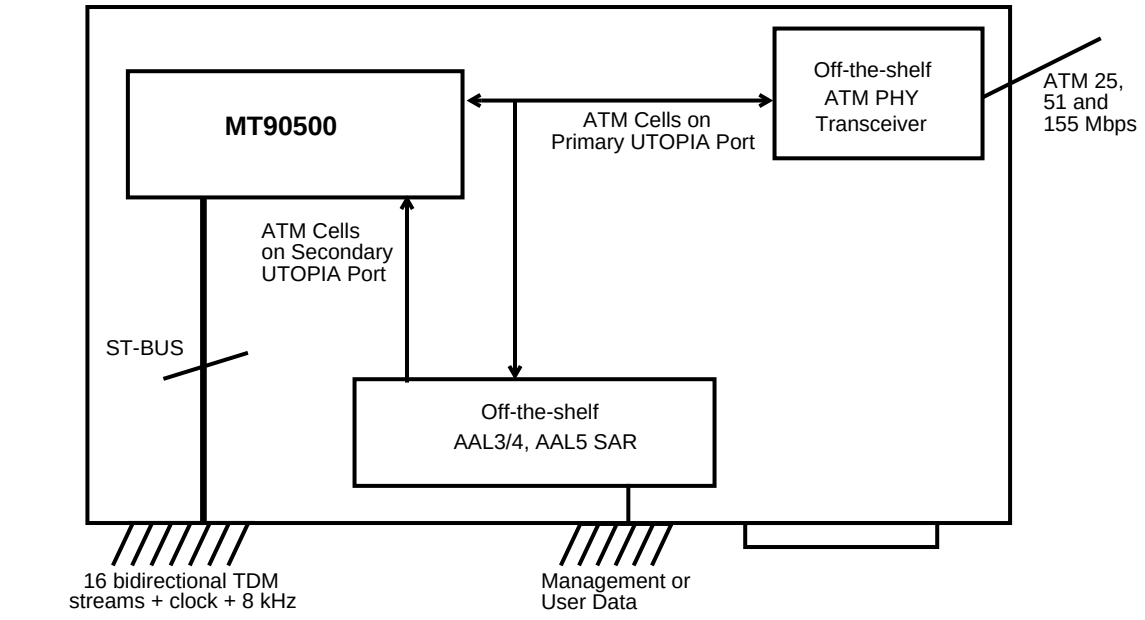


Figure 60 - Using the MT90500 with External SAR and ATM Links in a LAN

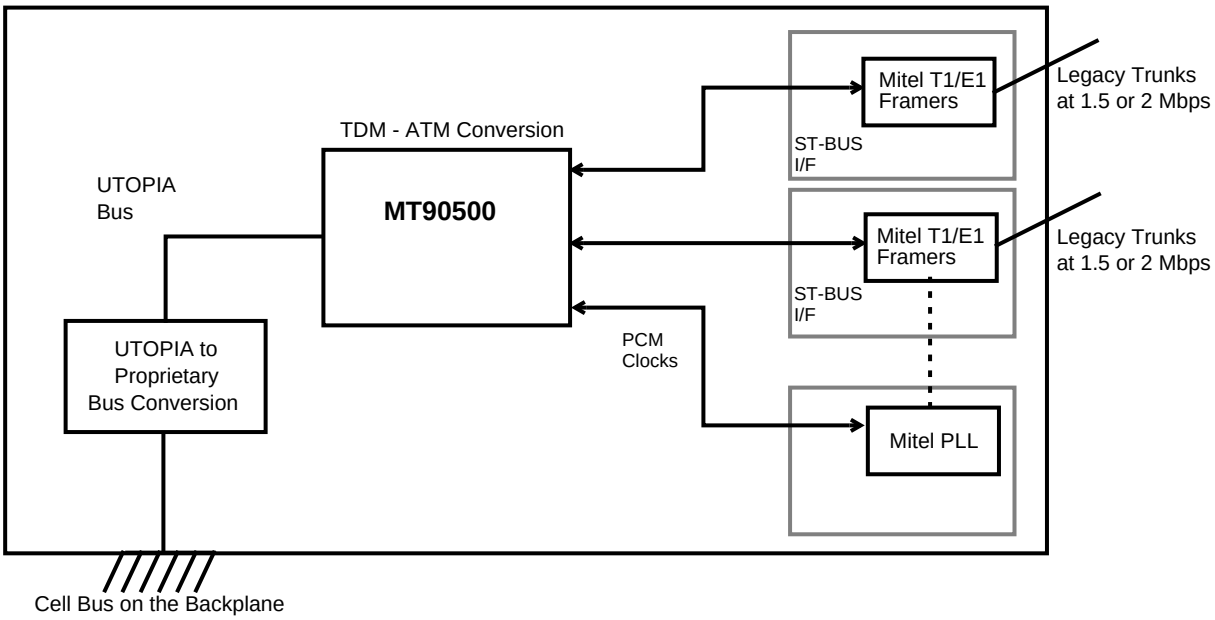


Figure 61 - Access Product using Internal High Speed Cell Bus on the Backplane

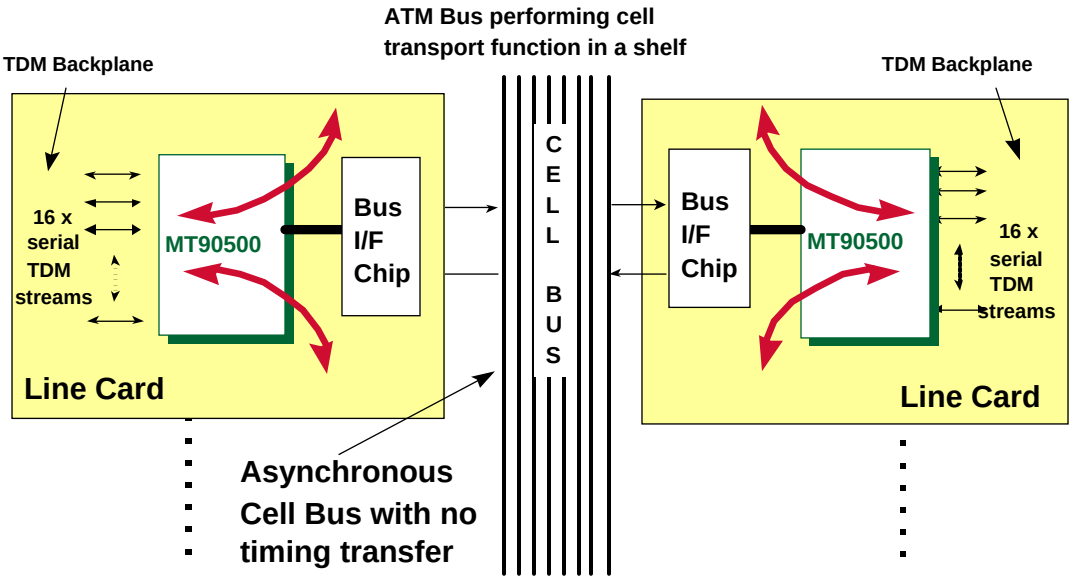


Figure 62 - TDM Traffic Transport Over a Cell Bus

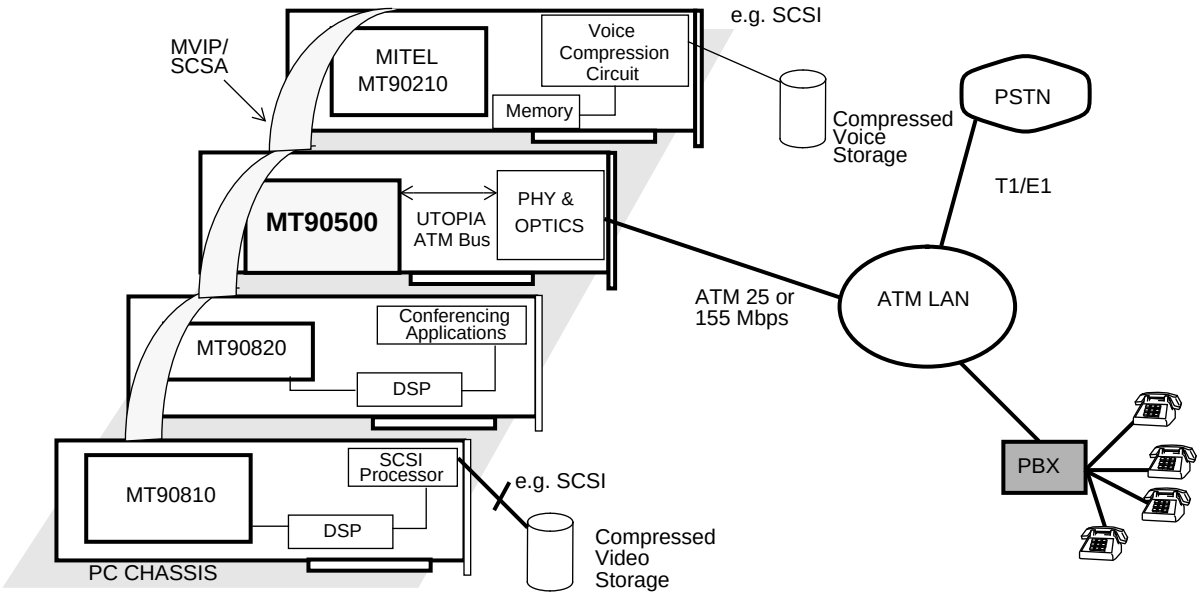


Figure 63 - Connecting CTI Platforms to ATM LANs

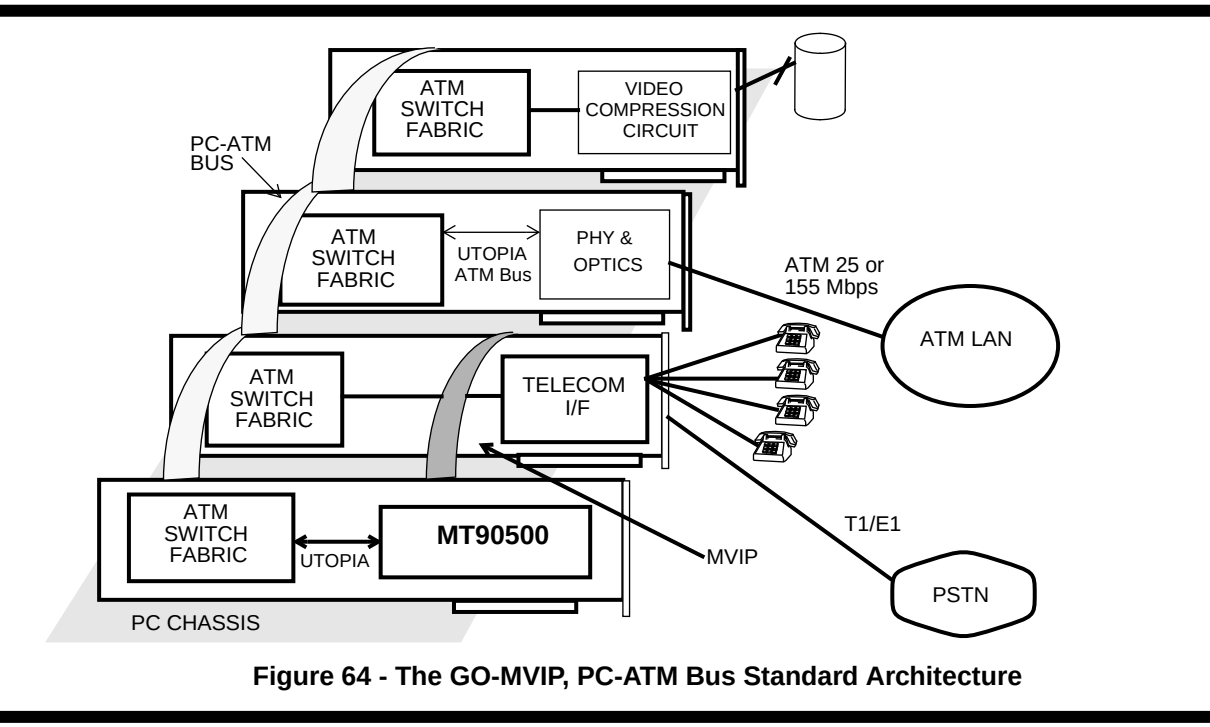


Figure 64 - The GO-MVIP, PC-ATM Bus Standard Architecture

7.3 TDM Clock Recovery Applications

By the nature of its function - carrying isochronous traffic over Asynchronous Transfer Mode networks - the MT90500 will be used in applications which require TDM clock synchronization. Further, these applications will often require the transfer or recovery of the isochronous TDM timing using the ATM link. There are several approaches to this TDM clock synchronization, both standardized and not-standardized. These clock synchronization methods include: synchronization to plesiochronous trunks, synchronization to the ATM physical layer, adaptive clock recovery, SRTS clock recovery, and allowing the TDM clocks to freerun.

The choice of clock synchronization method is dependent upon the application. Most standards documents which deal with this issue specify that the recovered clock should be synchronized to the most accurate clock available. The ITU-T Recommendation I.363.1 provides some guidance on these issues; see the “Convergence Sublayer” section, especially “Source clock frequency recovery method,” and Appendix II.

It is usually possible to provide intelligible voice connections using a freerunning clock, provided that the crystal accuracy is constrained to a few parts per million. Freerunning clocks are not recommended however, as relatively frequent frame slips (and accompanying data errors) are inevitable, and this is generally not acceptable for data going to the public network.

7.4 External Memory Space and Bandwidth Calculations

7.4.1 External Memory Space Requirements

This section provides a list of the control and data structures used by the MT90500 which are located in external memory. An estimation of the structure size is provided, assuming various scenarios: 256, 512, and 1024 TDM channels in both directions and from 16 to 1024 VCs. (In line with accepted usage for memory, here 1 Kbyte = 1024 bytes.)

Transmit Memory Requirements

Refer to Figure 19, “Overview of CBR Data Transmission Process,” on page 50.

A. TX Circular Buffer Control Structure

Two bytes of RAM are required for every TDM channel transmitted.

- 256 TDM channels 0.5 Kbyte
- 512 TDM channels 1 Kbyte
- 1024 TDM channels 2 Kbytes

B. Transmit Circular Buffers

64 bytes of RAM are required for every TDM channel transmitted.

- 256 TDM channels 16 Kbytes
- 512 TDM channels 32 Kbytes
- 1024 TDM channels 64 Kbytes

C. Transmit Event Scheduler

Assume either 1 scheduler, or all 3 schedulers in service. Assume the schedulers are composed of 47 frames (AAL1-SDT) and each frame contains 16 two-byte VC Pointer entries.

- 1 scheduler ~ 1.5 Kbytes
- 3 schedulers ~ 4.4 Kbytes

D. Transmit Control Structure

Each control structure begins with 12 bytes of control data, followed by 2 bytes of information for each TDM channel. All transmit control structures occupy an integer number of 16-byte blocks.

- 16 VCs (16 TDM channels per VC) 0.75 Kbyte (16 * ROUNDUP(12 + 16 * 2) = 768 bytes)
- 128 VCs (4 TDM channels per VC) 4 Kbytes (128 * ROUNDUP(12 + 4 * 2) = 4096 bytes)
- 1024 VCs (1 TDM channel per VC) 16 Kbytes (1024 * ROUNDUP(12 + 1 * 2) = 16384 bytes)

E. Transmit Data Cell FIFO holding 64 cells (Refer to Section 4.3.3.)

- 64 data cell structures at 64 bytes each 4 Kbytes

Sub-total external memory space requirements to support the TDM to ATM transmit process:

Minimum requirements (256 channels, 1 scheduler):	22.7 Kbytes
Maximum requirements (1024 channels, 3 schedulers):	90.4 Kbytes

Receive Memory Requirements

See Figure 30, “Overview of CBR Data Reception Process,” on page 64.

A. VC Look-up Table

Note: These numbers assume one-to-one mapping of look-up table entries to VCs. Larger “sparse” tables may be used in some applications, up to 128 Kbytes.

- 16 possible VCs 0.0625 Kbyte
- 128 possible VCs 0.5 Kbytes
- 1024 possible VCs 4 Kbytes

B. RX_SAR Control Structures

Each control structure begins with 12 bytes of control data, and is then followed by 2 bytes of information for each TDM channel. For the purposes of these calculations, all RX_SAR control structures are designed to occupy an integer number of 16-byte blocks.

- 16 VCs (16 TDM channels per VC) 0.75 Kbyte (16 * ROUNDUP(12 + 16 * 2) = 768 bytes)
- 128 VCs (4 TDM channels per VC) 4 Kbytes (128 * ROUNDUP(12 + 4 * 2) = 4096 bytes)
- 1024 VCs (1 TDM channel per VC) 16 Kbytes (1024 * ROUNDUP(12 + 1 * 2) = 16384 bytes)

C. Receive Circular Buffers

A 64-byte buffer provides 8 ms of buffering capability (1 byte = 125 µs) while a 1024-byte buffer provides up to 128 ms of buffering. In this example, we give sizes for a 64-byte and a 1024-byte (64 / 1024) buffer for each channel.

- 256 TDM channels 16 / 256 Kbytes
- 512 TDM channels 32 / 512 Kbytes
- 1024 TDM channels 64 / 1024 Kbytes

D. External Memory to Internal TDM Memory Structure

Four bytes of RAM are required for every TDM channel transmitted.

- 256 TDM channels 1 Kbyte
- 512 TDM channels 2 Kbytes
- 1024 TDM channels 4 Kbytes

E. Receive Data Cell FIFO holding 64 cells (Refer to Section 4.5.4.)

- 64 at 64 bytes each 4 Kbytes

Sub-total external memory space requirements to support the ATM to TDM receive process:

Minimum requirements (256 channels, 64-byte buffers): ~22 Kbytes

Maximum requirements (1024 channels, 1024-byte buffers): 1052 Kbytes

Total Memory Requirements

Total external memory size requirements to support both the TDM to ATM transmit process and the ATM to TDM receive process:

Minimum requirements: 44.7 Kbytes (256 X 64 kbps bidirectional channels with 16 VCs)

Maximum requirements: 1142.4 Kbytes (1024 X 64 kbps bidirectional channels with 1024 VCs)

Where the memory requirements are close to the physical size of the provisioned memory, the designer should pay special attention to what memory address boundaries some structures may not cross. (See Section 7.4.2.)

7.4.2 Memory Structure Summary

Table 94 - Summary of External Memory Structures

External Memory Structure	SIze (in bytes)	Start on Boundary	Do not cross boundary	Notes
TX Circular Buffer Control Structure	Min: 256 Max: 4096	Control structure must start on **512-byte** boundary: x0 0000 0000 Register 6040h: TXCBCSBASE = bits<20:9> of TX Circular Buffer Control Structure Base Address.	Control structures cannot cross an **8192-byte (8K)** boundary x0 0000 0000 0000 Therefore, to ensure that structure never crosses this boundary, start structure on a boundary equal to the structure size.	Structure size = # of entries * 2 bytes/entry.
TX Circular Buffers	64 (per TDM channel transmitted)	First buffer must start on a **512-byte** boundary: x0 0000 0000 Register 6044h: TXCBBASE = bits<20:9> of TX Circular Buffer Base Address.		Each subsequent buffer automatically starts on next 64-byte boundary.
Transmit Control Structures	Min: 14 Max: 256 (per VC)	Each control structure must start on a **16-byte** boundary: x 0000 Register 2040h: TXBASE = bits<20:16> of Transmit Control Structure Base Address. The address in the scheduler provides bits<15:4> of address.	Control structures cannot cross a **256-byte** boundary x 0000 0000	
Transmit Event Schedulers	Min: 16 Max: 16K (per scheduler - up to 3 can be configured)	Each scheduler must start on a **512-byte** boundary: x0 0000 0000 Register 2010h/2020h/2030h: SBASE = bits<20:9> of Scheduler Base Address.		Min. Size = 1 frame * 8 entries/frame * 2 bytes/entry. Typ. Size = 47 frames * 16 entries/frame * 2 bytes/entry. Max. Size = 256 frames * 32 entries/frame * 2 bytes/entry.
Look-Up-Table	Min: 1024 Max: 128K	The look-up table must start on a boundary equal to the **table size** = 2^(M+N+2) = #-of-entries * 4 bytes Register 401Eh: LUTBASE = bits<20:5> of pointer to start of look-up table. Register 4010h: M and N = number of LSBs from VPI and VCI, respectively, to be used in address.		Min. Size = 2^(8 + 2) = 1024. Max. Size = 2^(15 + 2) = 131072 = 128K. Requires external memory allocation of 2^(M + N + 2) bytes.

Table 94 - Summary of External Memory Structures

External Memory Structure	SIze (in bytes)	Start on Boundary	Do not cross boundary	Notes
External Memory to Internal Memory Control Structure	Min: 512 Max: 8192	Control structure must start on **512-byte** boundary: x0 0000 0000 Register 6042h: EIMCSBASE = bits<20:9> of External to Internal Memory Control Structure Base Address.	Control structures cannot cross an **8192-byte (8K)** boundary x0 0000 0000 0000 Therefore, to ensure that structure never crosses this boundary, start structure on a boundary equal to the structure size.	Structure size = # of entries * 4 bytes/entry.
RX Circular Buffers	Min: 64 Max: 1024 (one buffer per received TDM channel)	Buffers must start on boundary equal to **buffer size**: 64 - x00 0000 128 - x000 0000 256 - x 0000 0000 512- x0 0000 0000 1024 - x00 0000 0000 Number of unique bits provided differs in External to Internal Memory Control Structure: 64 bytes - bits<20:6> 128 bytes - bits<20:7> 256 bytes - bits<20:8> 512 bytes - bits<20:9> 1024 bytes - bits<20:10>		Buffer size is controlled by the External to Internal Memory Control Structure and the RX_SAR Control Structure.
RX_SAR Control Structures	Min: 14 Max: 256 (per VC)	Each control structure must start on a **16-byte** boundary: x 0000 Register 4000h: RXBASE = bits<20:18> of RX_SAR Control Structure Base Addresses. Look-up Table entry provides bits<17:4> of address.	Control structures cannot cross a **256-byte** boundary x 0000 0000	
Transmit Data Cell FIFO	Min: 1024 Max: 8192	FIFO must start on a **512-byte** boundary: x0 0000 0000 Register 2050h: TXFFBASE = bits<20:9> of Transmit Data Cell FIFO Base Address.	FIFOs cannot cross an **8192-byte (8K)** boundary x0 0000 0000 0000 Therefore, to ensure that FIFO never crosses this boundary, start FIFO on a boundary equal to the FIFO's size.	Each non-CBR cell occupies a 64-byte buffer within the FIFO. Min. Size = 16 cells * 64 bytes/cell. Max. Size = 128 cells * 64 bytes/cell. May be omitted.
Receive Data Cell FIFO	Min: 1024 Max: 8192	FIFO must start on a **512-byte** boundary: x0 0000 0000 Register 4020h: RXFFBASE = bits<20:9> of Receive Data Cell FIFO Base Address.	FIFOs cannot cross an **8192-byte (8K)** boundary x0 0000 0000 0000 Therefore, to ensure that FIFO never crosses this boundary, start FIFO on a boundary equal to the FIFO's size.	Each non-CBR cell occupies a 64-byte buffer within the FIFO. Min. Size = 16 cells * 64 bytes/cell. Max. Size = 128 cells * 64 bytes/cell. May be omitted.

7.4.3 External Memory Bandwidth Requirements

The following section provides estimated external memory bandwidth requirements to support the functionality of the MT90500, excluding negligible non-CBR traffic (i.e. data cells or OAM cells). The following scenarios are examined: 256, 512, and 1024 bidirectional TDM channels. The memory clock MEMCLK is tied to the input MCLK, which also clocks all internal processes, and also controls CPU access speed.

ATM Transmit Process Bandwidth

A. Access to TX Circular Buffer Control Structure.

One word read access is required per TDM channel every 4 frames. Thus, one double-word access can retrieve 2 TDM channels every 4 frames (500 µs):

(1 double-word read access / (2 channels * 500 µs)) * 'N' TDM channels = 1000 * 'N' accesses/s.

- 256 TDM channels 0.256 M accesses / s
- 512 TDM channels 0.512 M accesses / s
- 1024 TDM channels 1.024 M accesses / s

B. Access to the Transmit Circular Buffers.

One double word (32-bit) write access is required to transfer a TDM channel into a circular buffer every four frames (500 µs). As well, four additional read accesses are required to retrieve the data byte by byte:

((1 double-word write access + 4 half-word read accesses) / 500 µs) * 'N' TDM channels = 10000 * 'N' accesses/s.

- 256 TDM channels 2.56 M accesses / s
- 512 TDM channels 5.12 M accesses / s
- 1024 TDM channels 10.24 M accesses / s

C. Access to Transmit Event Schedulers.

Assuming that we have selected 16 VC Pointers (one word each) per frame, we require eight double-word read accesses per scheduler per frame (125 µs):

(8 double-word read accesses / 125 µs) * 'N' event schedulers = 64000 * 'N' accesses/s.

- 1 scheduler 0.064 M accesses / s
- 3 schedulers 0.192 M accesses / s

D. Transmit Control Structure Accesses.

Each cell transmitted requires three control double-word read accesses (for the twelve bytes of control data at the start of each Transmit Control Structure), one control double-word write access (to update the Current Entry, Sequence Number, and Circular Buffer Pointer fields of the Transmit Control Structure), as well as up to 24 double-word read accesses (to select up to 48 TDM Circular Buffer addresses per cell) to know which data to transfer, for a total of up to 28 memory accesses per cell transmitted. 256 TDM channels represent a rate of ~ 5.5 cells / 125 µs; 512 TDM channels represent a rate of ~11 cells / 125 µs; etc.

(28 double-word memory accesses * estimated cell arrival rate (per 125 µs) = 224000 * cell arrival rate.

* The case of one TDM channel per cell has been optimized to outperform the standards stated herein. The case of VCs having odd numbers of TDM channels is slightly worse than the number given.

- 256 TDM channels 1.232 M accesses / s
- 512 TDM channels 2.464 M accesses / s
- 1024 TDM channels 4.928 M accesses / s

Sub-total external memory access bandwidth requirements to support the TDM to ATM transmit process:

Minimum requirements: ~ 4.11 M accesses / sec

Maximum requirements: ~ 16.4 M accesses / sec

ATM Receive Process Bandwidth

A. Access to VC Look-up Table.

Assuming an overall inbound traffic rate of 25.6 Mbps, the External Memory to Internal TDM Memory Structure encounters a maximum of ~60,000 cells per second (i.e. (3.2 Mbytes/s) / (53 bytes/cell) = 60377.36 cells / s). Assuming an overall inbound traffic of 155.52 Mbps (again, 1M = 1 000 000), the External Memory to Internal TDM Memory Structure encounters ~400,000 cells per second (i.e. (19.44 Mbytes/s) / (53 bytes/cell) = 366792.45 cells / s). There is one double-word read access per cell.

- 25.6 Mbps ~ 0.06 M accesses / s
- 155.52 Mbps ~ 0.4 M accesses / s

B. RX_SAR Control Structure Accesses.

Each received cell requires three control double-word read accesses (for the twelve bytes of control data at the start of each RX_SAR Control Structure), one control double-word write access (to update the Current Entry and TDM Write Pointer fields of the RX_SAR Control Structure), as well as up to 24 double-word read accesses (to select up to 48 RX Circular Buffer Base Addresses per cell) to know which data to transfer, for a total of up to 28 memory accesses per cell transmitted. 256 TDM channels represent a rate of ~ 5.5 cells / 125 µs; 512 TDM channels represent a rate of ~11 cells / 125 µs; etc.

28 double-word read accesses * estimated cell arrival rate (per 125 µs) = 224000 * cell arrival rate.

- 256 TDM channels 1.232 M accesses / s
- 512 TDM channels 2.464 M accesses / s
- 1024 TDM channels 4.928 M accesses / s

C. Access to the Receive Circular Buffers.

One double-word (32-bit) read access followed by a double-word write access (to clear the underrun bit after the byte has been read) per TDM channel every four frames (500 µs). Four times as many accesses are required to transfer the data from the received cell to the circular buffer, byte per byte.

((1 double-word read access + 1 double-word write access + 4 half-word write accesses) / 500 µs * 'N' TDM channels = 12000 * 'N' accesses/s.

- 256 TDM channels 3.07 M accesses / s (5.63 M accesses / s)
- 512 TDM channels 6.14 M accesses / s (11.3 M accesses / s)
- 1024 TDM channels 12. 3 M accesses / s (22.5 M accesses / s)

D. Access to the External Memory to Internal TDM Memory Structure.

One double-word read access is required per TDM channel every 4 frames (500 µs):

(1 double-word read access / 500 µs) * 'N' TDM channels = 2000 * 'N' accesses/s.

- 256 TDM channels 0.512 M accesses / s
- 512 TDM channels 1.024 M accesses / s
- 1024 TDM channels 2.048 M accesses / s

Sub-total of external memory access bandwidth requirements to support the ATM to TDM receive process:

Minimum requirements: ~ 7.76 M accesses / s

Maximum requirements: ~ 29.9 M accesses /s

Total Bandwidth Requirements

Total of external memory access bandwidth requirements to support both the TDM to ATM transmit and the ATM to TDM receive process:

Minimum requirements: ~ 11.9 M accesses / s

Maximum requirements: ~ 46.3 M accesses /s

The above maximum requirement defines the theoretical minimum clock frequency the design must achieve to support 1024 X 64 kbps bidirectional channels with 1024 VCs. Assuming a 29% margin for CPU accesses, AAL0 cell processing, and random lost memory access efficiency, the MT90500 should be supplied with a master clock (MCLK) of 60 MHz to support 1024 X 64 kbps bidirectional channels with 1024 VCs. It is also recommended to select SSRAM to minimize turnaround cycles, for the greatest memory efficiency.

7.5 CBR Throughput Delay

Delay through the MT90500, from TDM bus to TDM bus, depends on a number of variables, not all of which are under the control of the designer. The following examples omit ATM network delay (transmission delay), TDM switching delay (caused by moving a TDM channel from time slot 0 to time slot 32, for instance) and CDV buffer delay (Avg. Lead of the RX Circular Buffer). The first example uses AAL1, n=1, fully-filled cells, the delay for which can be up to 66 frames (8.25 msec). This is due to the following factors:

```
  4  frames TX TDM Input Frame Buffer
  3  frames TX offset (TDM Write Pointer to TX_SAR Read Pointer)
 47  frames cell assembly (47 byte payload)
  8  frames RX Circular Buffer delay (Avg. Lead = 02h, = 8 frames)
  4  frames RX TDM Output Frame Buffer.
----
 66  frames
```

An example of minimum delay (applicable for n> 47, or n = partial-fill level) would be 16 frames (2 msec) as follows:

```
  4  frames TX TDM Input Frame Buffer
  3  frames TX offset (controlled by MT90500, could be as low as 1 or 2)
  1  frame cell assembly (#-of-TDM n > 47, or n = partial-fill level)
  4  frames RX Circular Buffer delay (Avg. Lead = 01h, = 4 frames)
  4  frames RX TDM Output Frame Buffer.
---
 16  frames
```

To these numbers, the designer may wish to add the application-specific delays: ATM network transmission delay, CDV buffer delay, and TDM switching delay.

7.6 Miscellaneous Applications

Figure 65 indicates how the MT90500 can be used as a payload switch. In such an application, TDM data received in the cell payload of one ATM VC can be transmitted from the MT90500 as the cell payload of a different ATM VC. Note that this constrains the Receive Circular Buffers to 64 bytes, which limits the CDV tolerance.

Figure 66 shows how the CORSIG/MC pins are used in an SCSA Message Channel application.

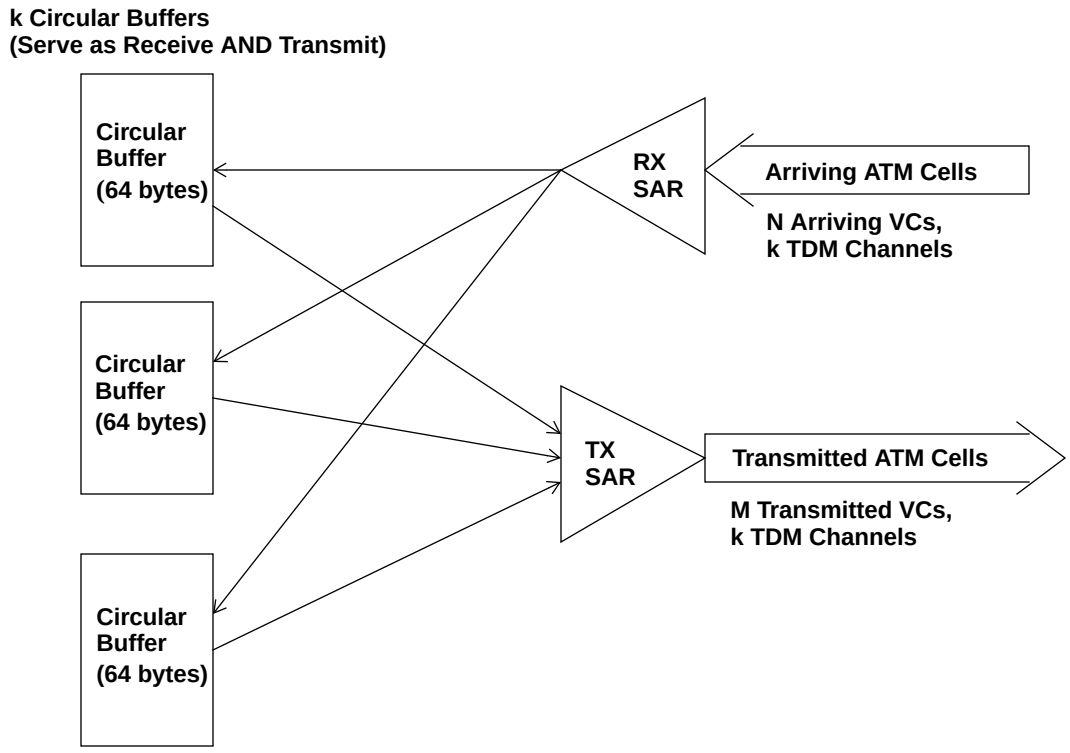


Figure 65 - TDM Payload Switching

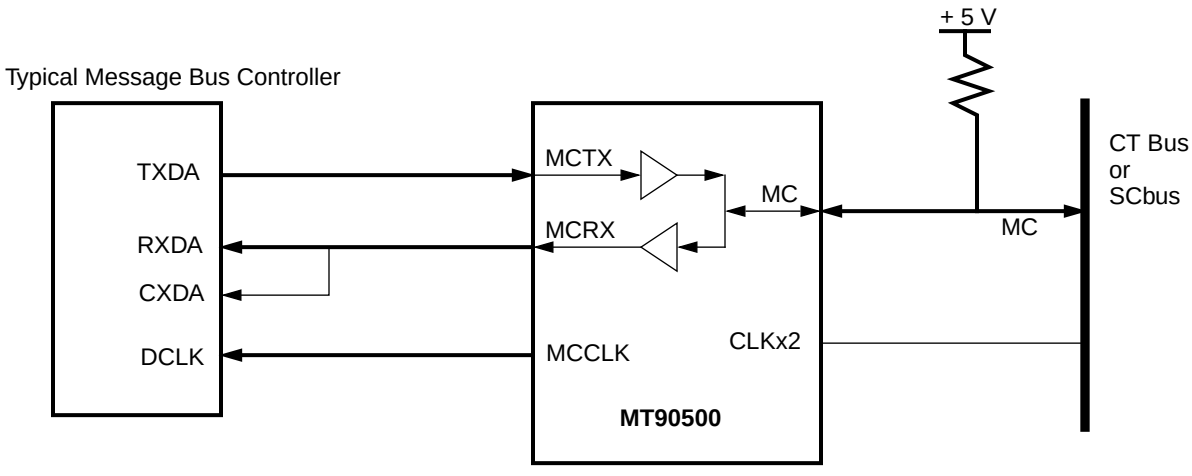
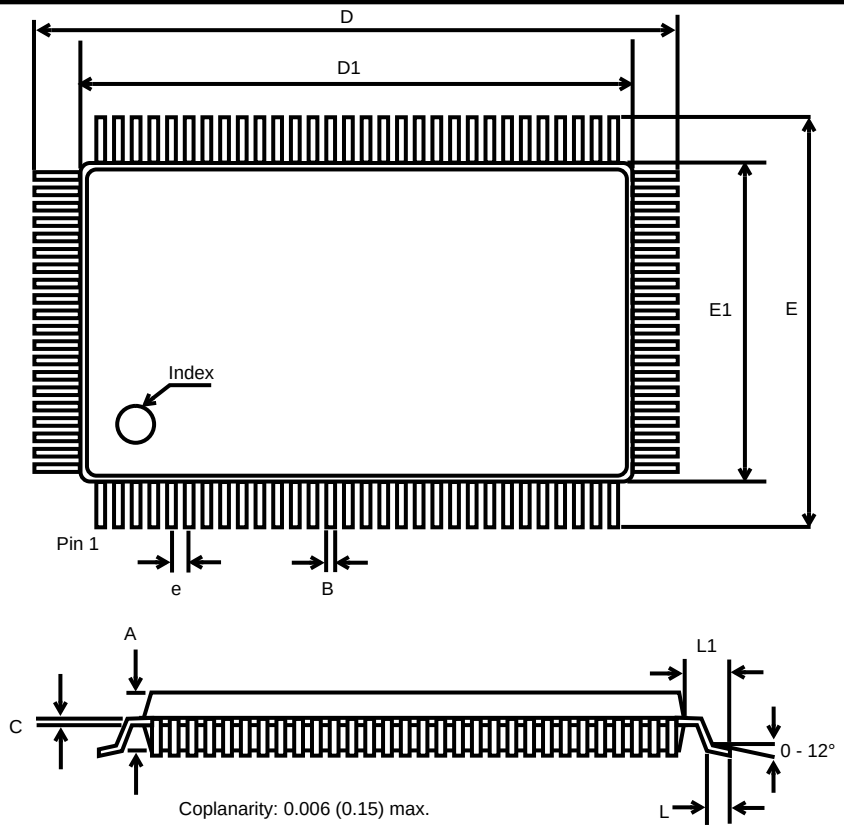


Figure 66 - SCSA Message Bus Application

8. Physical Specification



Dim	240-Pin	
	Min	Max
A	-	(4.1)
B	(0.17)	(0.27)
C	(0.09)	(0.2)
D	(34.4)	(34.8)
D1	(31.9)	(32.1)
E	(34.4)	(34.8)
E1	(31.9)	(32.1)
L	(0.45)	(0.75)
L1	(1.3 REF)	
e	(0.5 REF)	

Notes:
1) Not to scale
2) Dimensions in inches
3) (Dimensions in millimeters)
4) JEDEC Standard 3.9mm footprint: M0-112
5) PQFP-240 Package complies to JEDEC Standard MO-143

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